Technical Information Manual

Revision n. 0
7 February 1996

MOD. V513

16 CHANNEL PROGRAMMABLE I/O REGISTER

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1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The model V513 is a 1-unit wide VME module that implements a 16 channel general purpose I/O module.

Each of the 16 channels can be programmed as **Input** or **Output** independently and can work in **Positive** or **Negative** logic.

Inputs and Outputs can be enabled via VME (**Transparent** Mode) or by an external Strobe signal (**Externally Strobed** Mode).

The external strobe input (STB) is high impedance and is provided with two bridge connectors for daisy chaining.

Each channel can also work in **Glitched** Mode; in this operating mode a positive or negative transition of an input signal can be memorized in the Input Register.

The channels' logic diagram is shown in fig 1.1.

For each channel a LED has been placed on the Front Panel to signal the I/O operation mode of the channel.

The module houses a fully programmable VME RORA INTERRUPTER[1] that generates a VME interrupt when one of the bits of the Input register becomes true. The bit pattern is programmable via a Mask register (Int Mask register). Moreover it is possible to generate the VME interrupt as a consequence of an external strobe.

The module V513 is an A24/A32 D16 VME slave; its Base address is fixed by 6 internal rotary switches. A front panel LED (DTACK) lights up each time the module generates the VME signal DTACK.

The Model uses the P1 and P2 connector of VME and the auxiliary connector for the backplane of the CERN V430[2] VMEbus crate (Jaux Dataway).

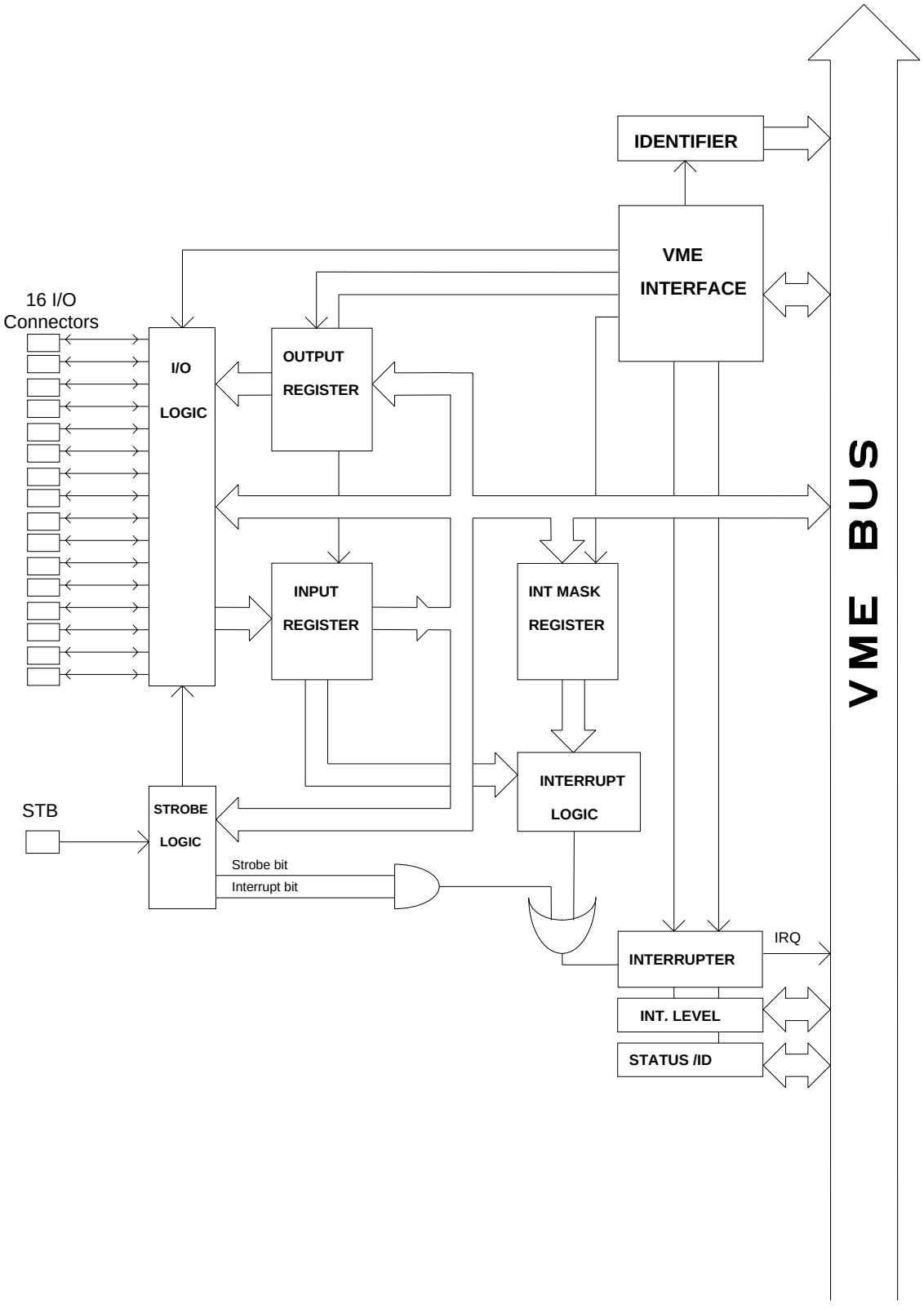


fig. 1. 1 : Mod. V513 block diagram.

2. SPECIFICATIONS

2.1. PACKAGING

1-unit wide VME unit. Height: 6U.

2.2. EXTERNAL COMPONENTS

CONNECTORS

- No.16, " 0..15", LEMO 00 type, 50 Ω impedance; for the 16 input/output channels.
- No.2, "STB", LEMO 00 type 50 Ω impedance; two bridge connectors (for daisy chaining) for the Strobe input signal.

LEDs

- No.1, "DTACK", green; VME Selected; it lights up during a VME access.
- No.16, "I/0", red; signalling the I/O direction of each channel (ON = Input).

2.3. INTERNAL COMPONENTS

(refer to fig.2.2)

SWITCHES

- No.6, rotary switches for the module VME Base address selection.

2.4. POWER REQUIREMENTS

+ 5 V	1.8 A
- 5 V	250 mA

2.5. CHARACTERISTICS OF THE SIGNALS

I/O CHANNELS:	std. NIM logic levels 50 Ω impedance. minimum width (Glitched mode): 10 ns.
STB(1):	std. NIM level, high impedance; max. frequency: 30 MHz; duty cycle: 50% minimum hold time: 25 ns; minimum set-up time: 25 ns.

(1) This input is high impedance and is provided with two bridge connectors for daisy chaining. Note that the chain has to be terminated on 50 Ω on the last module; the same is needed also if one module only is used, whose input has thus to be properly matched.

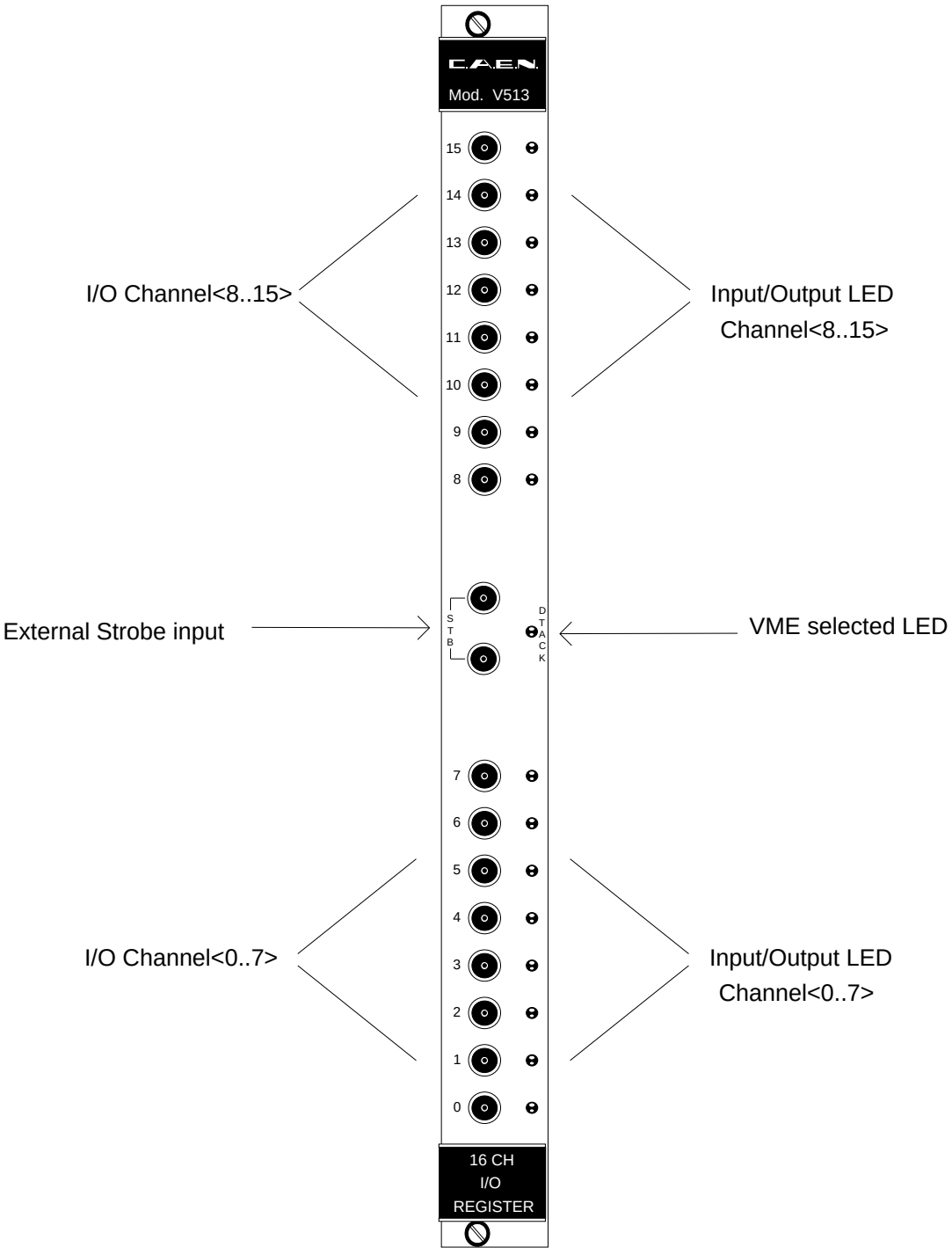


fig. 2. 1 : **Mod. V513 Front Panel**.

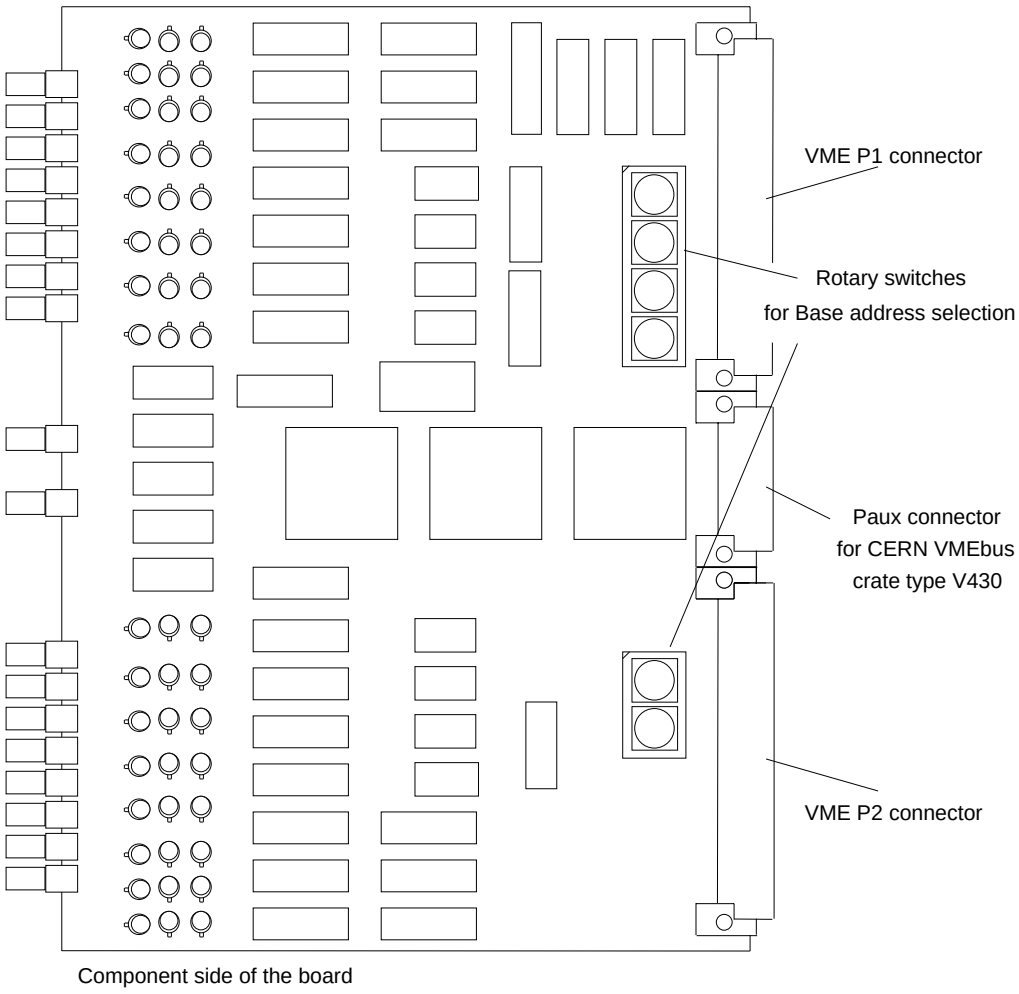


fig. 2. 2 : Mod. V513 components locations.

3. OPERATING MODES

3.1. INTRODUCTION

The Mod. V513 is a 16 Channels general purpose I/O module; each channel can be configured independently via 16 Status registers programmable via VME (Base address + %10..Base address + %2E).

Two 16 bit registers (Input and Output register) contains the channels' data. If a channel is configured as Output, the corresponding bit of the Output register is transferred to the corresponding I/O connector; while the corresponding bit of the Input register contains the channel Input data (If the channel is configured as Output, the Input register bit contains the Output Register bit value).

The two registers are accessible via VME (Base address + %04 read: Input register; Base address + %04 write: Output register).

Inputs and Outputs can be enabled by VME or by the external Strobe signal STB. A 3 bit register (Strobe register Base address +%06) accessible via VME controls the Strobe operations (polarity, interrupt generation) and allows to store an occurred STB pulse.

A 16 bit register (Int Mask register: Base address + %08) permits to set a mask to the Input register bits so that the VME interrupt is generated whenever almost one of the masked bit becomes true.

3.2. STROBE CONFIGURATION

The Output transferring and Input storing can be enabled by sending the external signal STB.

The Strobe register (Base address +%06) is a 3 bit register that allows:

- to set the STB polarity (Positive/Negative);
- to enable or not the VME interrupt generation as a consequence of an STB transition;
- to store an occurred STB transition.

The following table shows the functional characteristics corresponding to the status of the individual bits of the Strobe register:

Strobe reg. bit	Function	Meaning
bit 0	Polarity	0 = Positive 1 = Negative
bit 1	Interrupt	0 = STB transition does not cause a VME interrupt 1 = STB transition causes a VME interrupt (*)
bit 2	Strobe bit (**)	1= STB transition occurred 0 = no STB transition

(*) If the Interrupt level is different from 0.

(**) this bit is read-only.

The bit<2> is set to 1 if a STB transition occurs (the active edge is determined by the STB polarity). This bit is cleared by the following operations:

- By accessing in write via VME the address Base + %44 (Clear Strobe);
- By accessing in write via VME the address Base + %42 (Module reset);
- By generating the VME signal SYSRES.

The Module reset operation and the generation of the signal SYSRES clears also the other two bits of the Strobe register.

The STB input is high impedance and is provided with two bridge connectors for daisy chaining.

Note that since the STB is an high impedance input, the chain has to be terminated on 50 ohm on the last module; the same is needed also if one module only is used, whose input has thus to be properly matched.

3.3. CHANNEL CONFIGURATION

Each channel is equipped with a 4 bit Status register that controls the various channel configurations; through these registers it is possible to select:

- The channel direction (Input/Output) Status reg.<0>;
- The channel polarity (Positive/Negative) Status reg.<1>;
- The channel transfer mode (Transparent/Externally Strobed) Status reg.<3>.
- The channel input mode (Normal/Glitched) Status reg.<2>.

The following table shows the functional characteristics corresponding to the status of the individual bits of the Status registers:

The Status registers are available at VME addresses Base + %10 ... Base + %2E.

Status reg. bit	**Function**	**Meaning**
bit 0	Direction	0 = Output 1 = Input
bit 1	Polarity	0 = Negative logic 1 = Positive logic
bit 2	Input mode(*)	0 = Glitched mode 1 = Normal mode
bit 3	Transfer mode	0 = Transparent 1 = Externally strobed

(*) this bit is forced to 1 if the channel is configured as Output or If the channel is configured as input with Transfer mode = Externally strobed.

The following figure shows the structure of the V513 I/O channels; (the signals RD_INPUT_REG and WR_OUT_REG are generated by the VME interface).

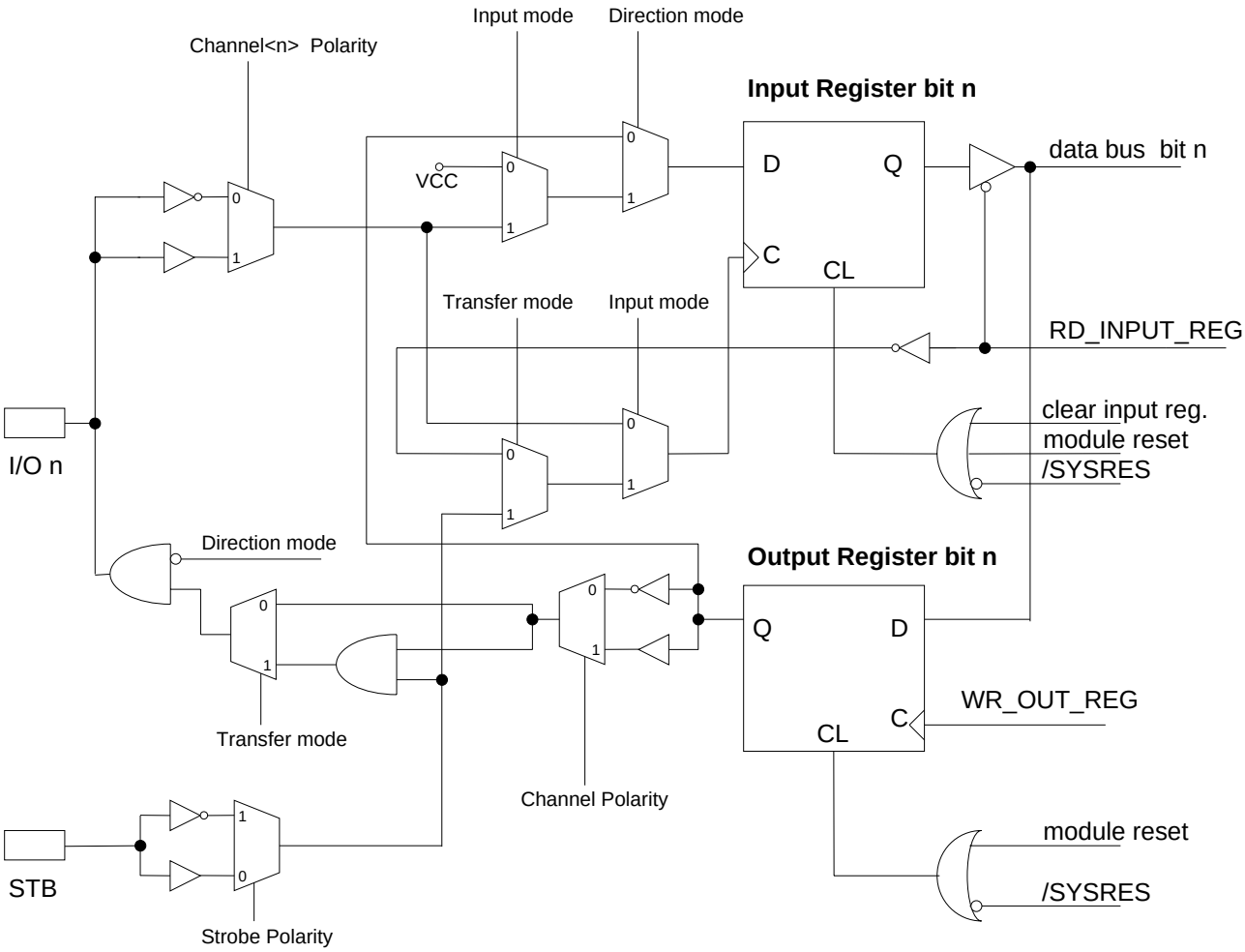


fig 3. 1 : Mod. V513 channel structure

3.3.1. INPUT CONFIGURATION

If the channel<n> is configured as Input, the data present on the I/O connector<n> is stored in the bit<n> of the Input register. The storage operation is controlled by the other bits of the Channel<n> Status register. The corresponding I/O LED is On.

3.3.2. OUTPUT CONFIGURATION

If the channel<n> is configured as Output, the data contained in the bit<n> of the Output register is transferred to the I/O connector<n> in one of the modes selected through the Transfer mode bit of the Channel<n> Status register. The corresponding I/O LED is Off.

In this case the bit<2> of the Status register (Input mode) is forced to 1, and in the bit<n> of the Input register it is stored the value written in the nth bit of the Output register.

3.3.3. POLARITY

The polarity bit controls the working logic of the channel.

3.3.4. TRANSPARENT TRANSFER MODE

In the Transparent mode the Input channels and the Output channels are enabled via VME.

INPUT
If the channel<n> is configured as Input, the data present on the I/O connector<n> is stored in the bit<n> of the Input register at the beginning of the VME read cycle of the Input register.
OUTPUT
If the channel<n> is configured as Output, the value stored in the bit<n> of the Output register is transferred to the I/O connector as soon as the write Output register operation is performed.

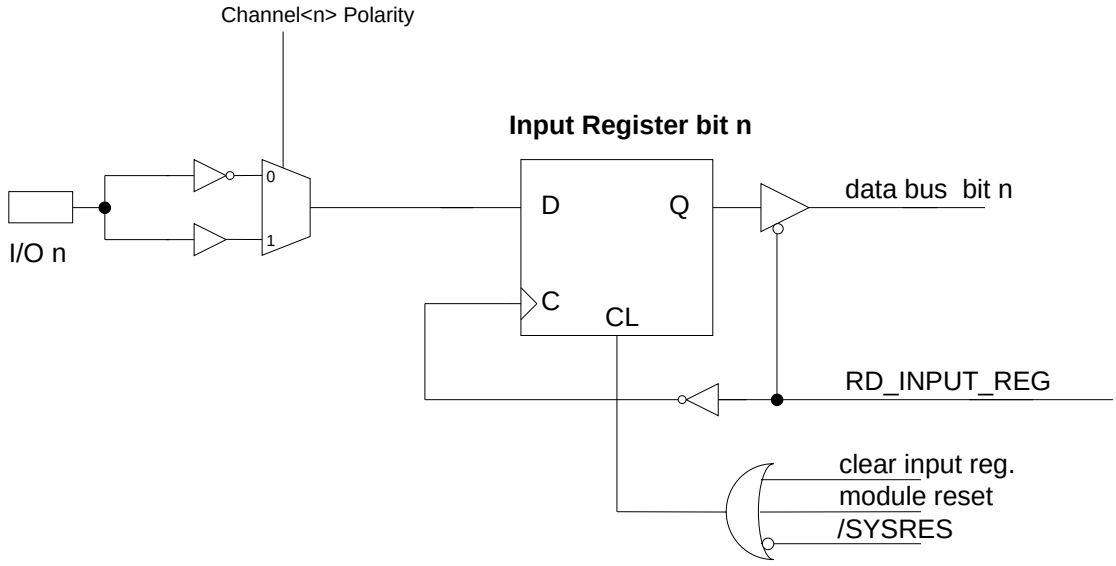


fig 3. 2: Channel<n> configured as Input, Transparent, Normal.

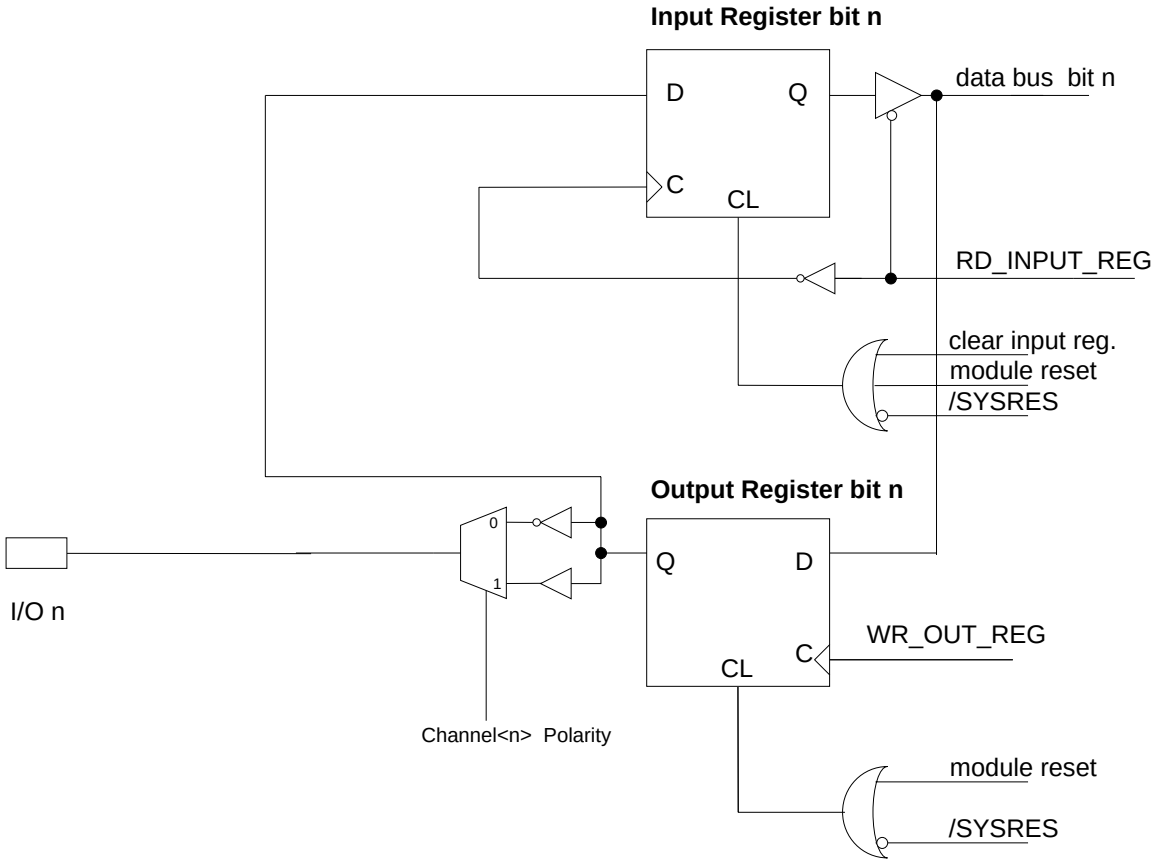


fig 3. 3 : Channel<n> configured as Output,Transparent.

3.3.5. EXTERNALLY STROBED TRANSFER MODE

In the Externally Strobed mode the Input channels and the Output channels are enabled via the external signal STB.

Via the Strobe register it is possible to select the active polarity of this signal.

INPUT
If the channel<n> is configured as Input, the data present on the I/O connector<n> is stored in the bit<n> of the Input register on a transition of the STB signal. The active transition (rising or falling edge) is determined by the selected STB polarity.

OUTPUT
If the channel<n> is configured as Output, the value stored in the bit<n> of the Output register is transferred to the I/O connector if STB is true. The active level is determined by the selected STB polarity.

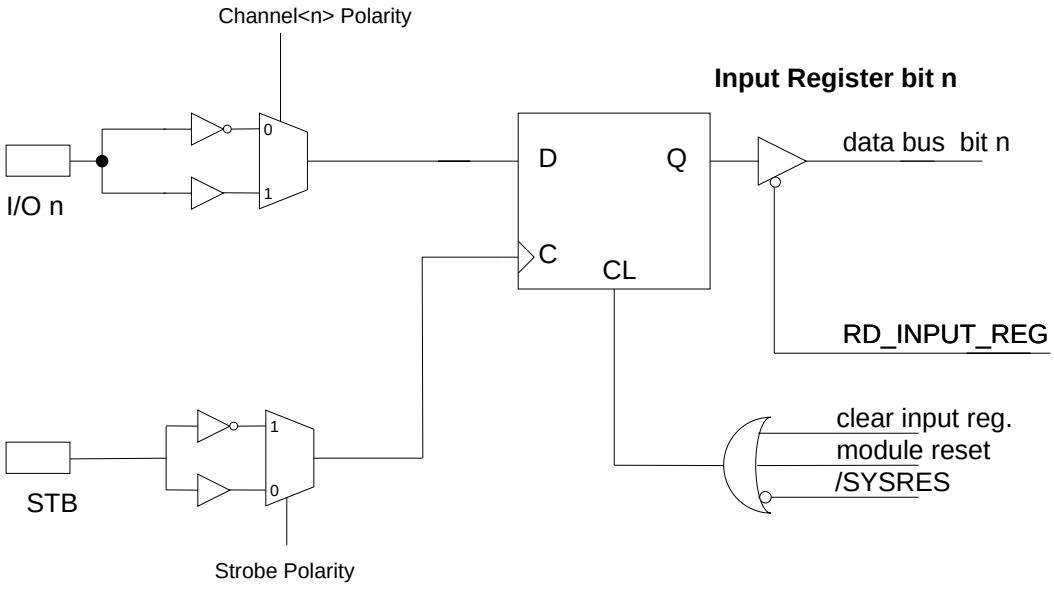


fig 3. 4 : Channel<n> configured as Input, Externally Strobed.

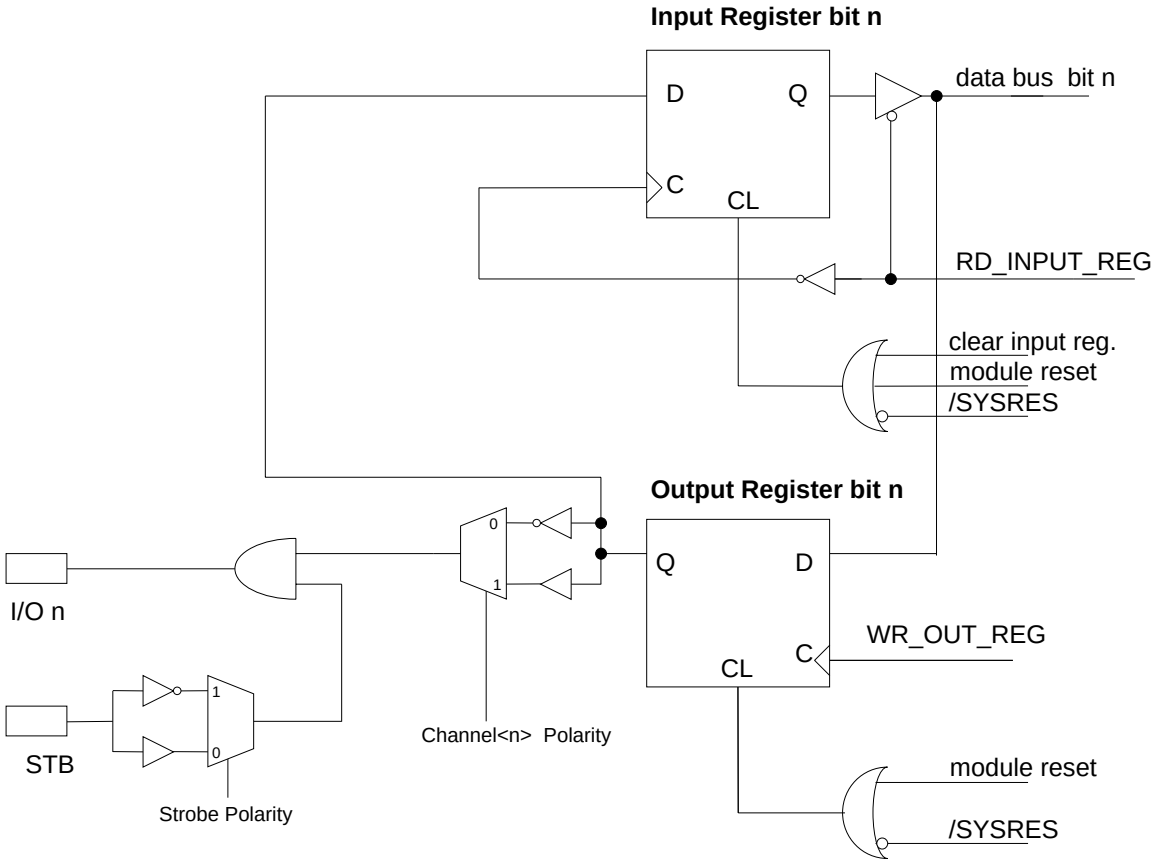


fig 3. 5 : Channel<n> configured as Output, Externally Strobed.

3.3.6. NORMAL INPUT MODE

If the channel<n> is configured as Input with Normal input mode, the data present on the I/O connector<n> is stored in the bit<n> of the Input register in one of the modes selected via the Transfer mode bit of the Channel<n> Status register.

This means that the Input register is configured as a D type Flip Flop with the D input connected to the I/O signal, and the clock input connected to the STB signal (Externally Strobed) or to a RD_INPUT_REG signal (Transparent mode).

3.3.7. GLITCHED INPUT MODE

This option is available only if the channel is configured as

- Input.
- Transfer mode = Transparent.

If the channel<n> is configured as Input, Transparent, Glitched, a positive or negative transition (selected via the channel Polarity) sets to 1 the bit<n> of the Input register.

This means that the Input register is configured as a D type Flip Flop with the D input connected to VCC, and the clock input connected to the I/O signal (see figures below).

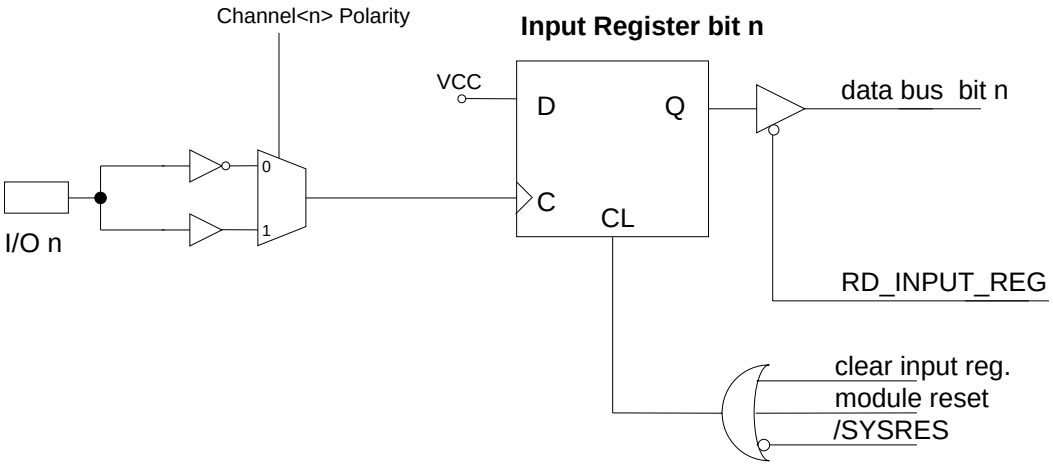


fig 3. 6 : Channel<n>configured as Input, Glitched.

3.3.8. MODULE CONFIGURATION

At power-on the 16 channels assume the default configuration: Status reg. values = %7:

- Direction = Input;
- Polarity = Positive;
- Input mode = Normal;
- Transfer mode = Transparent.

It is possible to set all the channels to the default configuration in these ways:

- By accessing in write via VME the address Base + %46 (Initialize Status registers);
- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

3.4. INPUT REGISTER CLEAR

The Input register is cleared in the following cases:

- By accessing in write via VME the address Base + %48 (Clear Input register);
- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

3.5. MODULE RESET

The module reset causes the following operations:

- All the channels assume the default configuration.
- the Input register is cleared;
- the Output register is cleared;
- the Interrupt level register is cleared (Interrupt disabled);
- the Int Mask register is cleared;
- the Strobe register is cleared.

The module reset is performed in these cases:

- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

3.6. INTERRUPT GENERATION

The operations of the V513 VME INTERRUPTER are fully software programmable; via VME it is possible:

- to set the VME interrupt level;
- to program the VME interrupt vector (STATUS/ID).
- to enable/disable the VME interrupt generation on an external STB transition;
- to enable/disable the VME interrupt generation for each bit of the Input register.

The VME INTERRUPTER generates a VME interrupt in these cases:

- whenever one enabled bit of the Input register becomes true;
- whenever the Strobe bit of the Strobe register becomes true (if enabled);

the Int Mask register allows to enable/disable the bits of the Input register: one bit of the Input register is enabled if it is masked via the Int Mask register (if the correspondig bit is set to 1).

That is, If the bit<n> of the Int Mask register is set to 1, a VME interrupt is generated when the bit <n> of the Input register becomes true,

Likewise, if the Interrupt bit of the Strobe register is set to 1, a VME interrupt is generated when the Strobe bit becomes true, i.e. when a STB transition is detected.

3.7. V430 BACKPLANE

The model V513 requires the backplane of the VMEbus crates type V430 [2] because the I/O section (NIM/TTL transceiver) make intensive use of the - 5.2 V power.

This backplane (VMEbus BIN type V431, see [2] § 2) is a monolithic printed circuit board that provides the VMEbus standard J1 and J2 dataway and a third dataway (named "Jaux") which is not foreseen by the VME standard.

The Jaux dataway provides some signals, the -5.2 V and -2 V requested by fast ECL logic front end modules and the +15 V and -15 V rails. This dataway is situated in the free space available between J1 and J2.

4. VME INTERFACE

4.1. ADDRESSING CAPABILITY

The module works in A32/A24 mode. This means that the module address must be specified in a field of 32 or 24 bits. The Address Modifiers code recognized by the module are:

AM=%39:	standard user data access
AM=%3D:	standard supervisor data access
AM=%09:	extended user data access
AM=%0D:	extended supervisor program access

The module's Base Address is fixed by 6 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 4.1).

The Base Address can be selected in the range:

% 00 0000 <-> % FF FF00	A24 mode
% 0000 0000 <->% FFFF FF00	A32 mode

The Base Address reserves in this way a page of 256 bytes for the module. The address map of the page is shown in table 4.1.

4.2. DATA TRANSFER CAPABILITY

The V513 registers are accessible in D16 mode;

Table 4.1: Address Map for the Mod. V513

ADDRESS	REGISTER/CONTENT	TYPE
Base + %FE	Version & Series	read only
Base + %FC	Manufacturer & Module Type	read only
Base + %FA	Fixed code	read only
Base + %50...Base + %F8	Reserved	
Base + %48	Clear Input register	write only
Base + %46	Initialize Status registers	write only
Base + %44	Clear Strobe bit	write only
Base + %42	Module Reset	write only
Base + %40	Clear VME Interrupt	write only
Base + %30...Base + %3E	Reserved	
Base + %2E	Channel15 Status register	read/write
Base + %2C	Channel14 Status register	read/write
Base + %2A	Channel13 Status register	read/write
Base + %28	Channel12 Status register	read/write
Base + %26	Channel11 Status register	read/write
Base + %24	Channel10 Status register	read/write
Base + %22	Channel9 Status register	read/write
Base + %20	Channel8 Status register	read/write
Base + %1E	Channel7 Status register	read/write
Base + %1C	Channel6 Status register	read/write
Base + %1A	Channel5 Status register	read/write
Base + %18	Channel4 Status register	read/write
Base + %16	Channel3 Status register	read/write
Base + %14	Channel2 Status register	read/write
Base + %12	Channel1 Status register	read/write
Base + %10	Channel0 Status register	read/write
Base + %0E..Base + 0%A	Reserved	
Base + %08	Int Mask register	read/write
Base + %06	Strobe register	read/write
Base + %04	Input register	read only
Base + %04	Output register	write only
Base + %02	Interrupt Level register	read/write
Base + %00	Interrupt Vector register	read/write

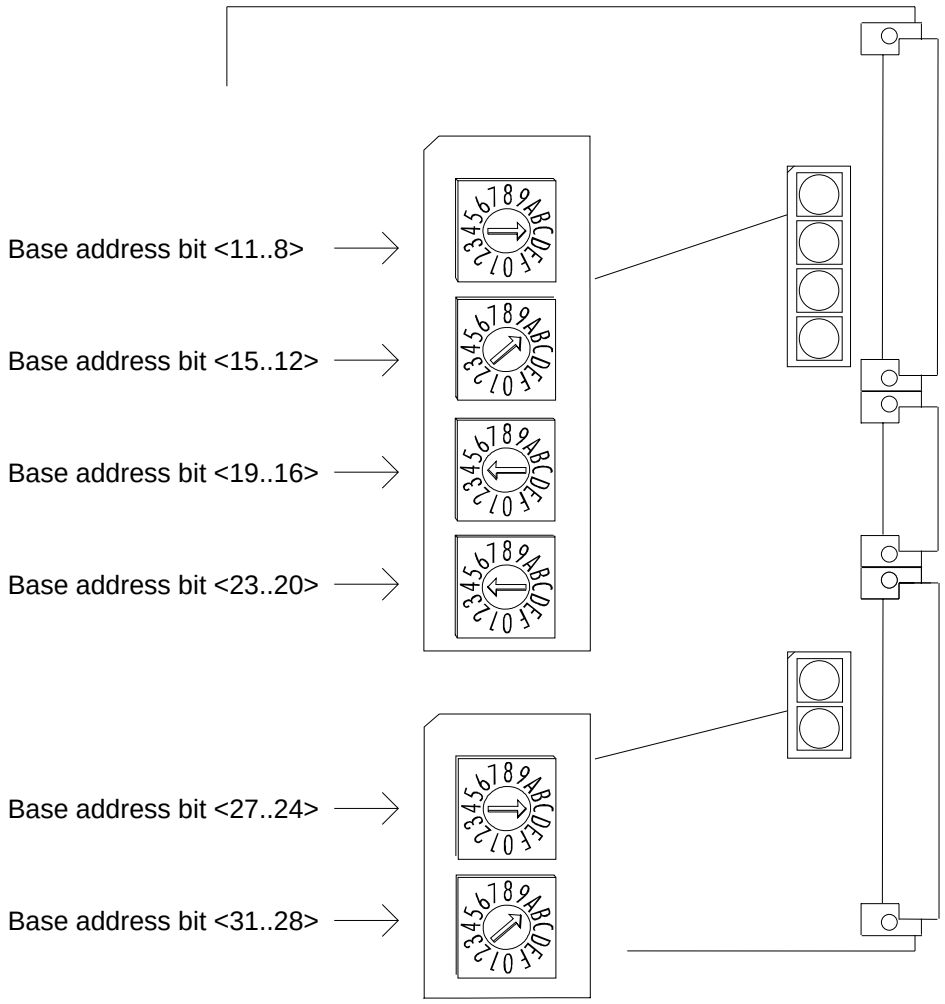


fig. 4. 1 : Mod. V513 Base address setting.

4.3. MODULE IDENTIFIER WORDS

(Base address + %FA ,+%FC, +%FE read only)

The Three words located at the highest address on the page are used to identify the module as shown in figure 4.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
%FA Fixed code								%F5 Fixed code								Base + % FA

fig. 4. 2 : Module identifier words.

At the address Base + % FA the two particular bytes allow the automatic localization of the module.

For the Mod. V513 the word at address Base + % FC has the following configuration:

Manufacturer N°= 000010 b

Type of module = 0000110010 b

The word located at the address Base + %FE identifies the single module via the module's serial number and any change in the hardware, (for example the use of faster logic) will be shown by the Version number.

4.4. CLEAR DATA REGISTER

(Base address + %48 write only)

A VME write access to this location clears the Input register.

4.5. INIZIALIZE STATUS REGISTERS

(Base address + % 46 write only)

A VME write access to this location sets all the channels to the default configuration. (Status reg. values = %7); all the channels are configured with:

- Direction = Input;
- Polarity = Positive;
- Input mode = Normal;
- Transfer mode = Transparent.

4.6. CLEAR STROBE BIT

(Base address + %44 write only)

A VME write access to this location clears the bit 2 of the Strobe register (Strobe bit).

4.7. MODULE RESET

(Base address + % 42 write only)

A VME write access to this location produces a module reset , this causes the following operations:

- All the channels assume the default configuration.
- the Input register is cleared;
- the Output register is cleared;
- the Interrupt level register is cleared (Interrupt disabled);
- the Int Mask register is cleared;
- the Strobe register is cleared.
- the VME interrupt request (if asserted), is removed.

4.8. CLEAR VME INTERRUPT

(Base address + % 40 write only)

A VME write access to this location removes the VME interrupt request (if asserted), (RORA INTERRUPTER).

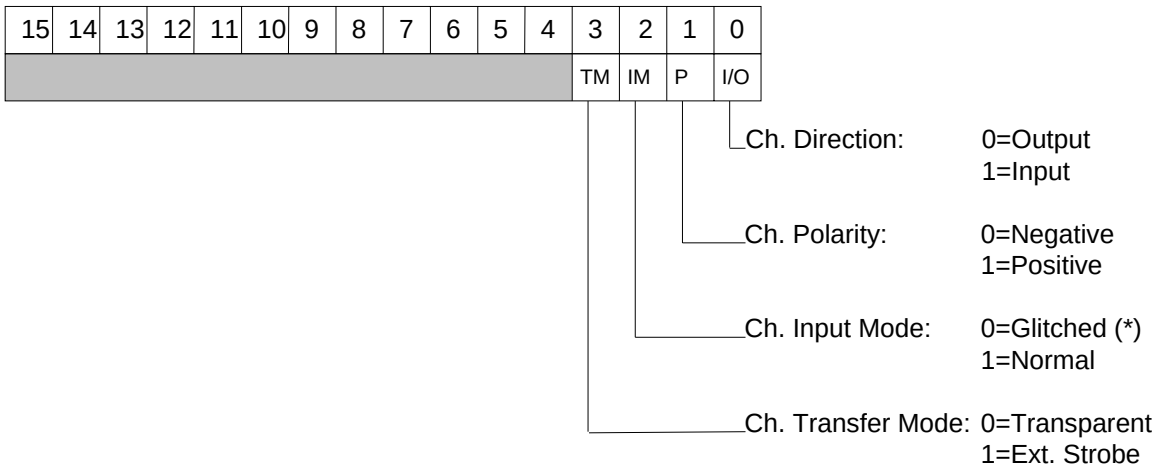
4.9. CHANNELS STATUS REGISTERS

(Base address + % 10...Base address + %2E r/w)

These are the 16 registers that control the channels configurations. (Bits 4 to 15 are unused and are read as "one" on the VME data bus).

All the 16 registers assume the default configuration (register content = %7) after one of the following operation:

- By accessing in write via VME the address Base + %46 (Initialize Status registers);
- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.



(*) This bit is forced to 1 if the channel is configured as Output or if the channel. is configured as Input with Transfer mode = Externally Strobed.

fig. 4. 3 : Channel Status register.

4.10. INT MASK REGISTER

(Base address + % 08 r/w)

This register allows to enable/disable the interrupt generation for each bit of the Input register.

If o bit of the Mask register is set to 1, the correspondig bit of the Input register is enabled to generate the VME interrupt when the bit itself becomes true.

The Int Mask register is cleared in the following cases:

- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M A S K < 15..0 >															

fig. 4. 4 : Int Mask register.

4.11. STROBE REGISTER

(Base address + % 06 r/w)

This register controls the Strobe operations. (Bits 3 to 15 are unused and are read as "one" on the VME data bus).

The bit 2 (Strobe bit) is read only, and it is set to 1 if a STB transition occurs. (the active edge is determined by the STB polarity). This bit is cleared by the following operations:

- By accessing in write via VME the address Base + %44 (Clear Strobe bit);
- By accessing in write via VME the address Base + %42 (Module reset);
- By generating the VME signal SYSRES.

(The Module reset operation and the generation of the signal SYSRES clears all the bits of the register).

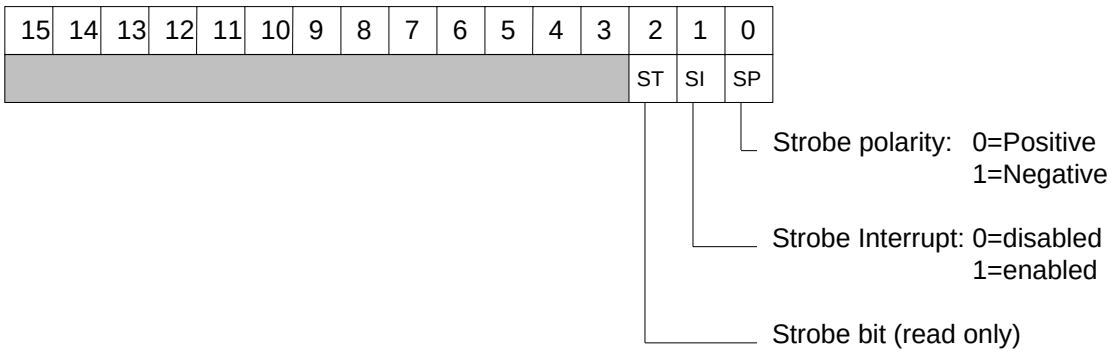


fig. 4. 5 : Strobe register.

4.12. INPUT REGISTER

(Base address + % 04 read only)

This 16 bit register contains the 16 channel Input data; each bit has an independent storage capability as explained in the § 3.3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNEL INPUT <15..0>															

fig. 4. 6 : Input register.

The Input register is cleared in the following cases:

- By accessing in write via VME the address Base + %48 (Clear Input register);
- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

4.13. OUTPUT REGISTER

(Base address + % 04 write only)

This 16 bit register contains the Output channels data; each bit can be transferred to the corresponding I/O connector as explained in § 3.3.

The Output register is cleared in the following cases:

- By accessing in write via VME the address Base + %42 (Module Reset);
- By generating the VME signal SYSRES.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNEL OUTPUT <15..0>															

fig. 4. 7 : Output register.

4.14. INTERRUPT LEVEL REGISTER

(Base address + %02 r/w)

The 3 LSB of this register contain the value of the interrupt level. (Bits <15..3> are unused and are read as "one" on the VME data bus).

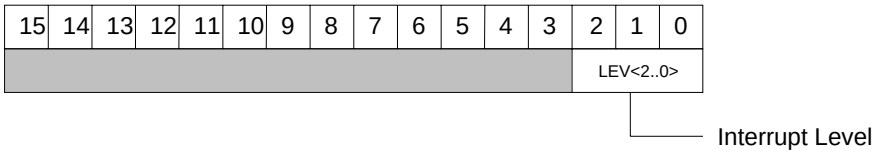


fig. 4. 8 : Interrupt Level register.

4.15. INTERRUPT VECTOR REGISTER

(Base address + %00 r/w)

The value stored in this register is the STATUS/ID that the V513 INTERRUPTER places on the VME data bus during the interrupt acknowledge cycle. (Bits 8 to 15 are unused and are read as "one" on the VME data bus).

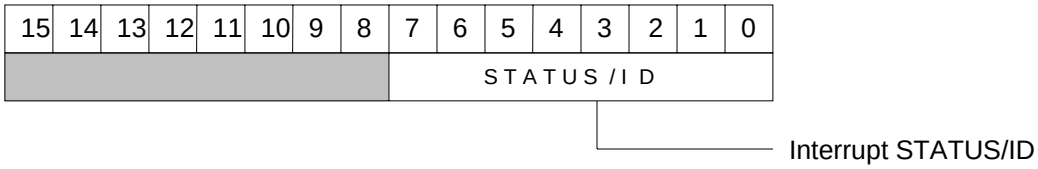


fig. 4. 9 : **Interrupt Vector register.**

5. MOD. V513 INTERRUPTER

5.1. INTERRUPTER CAPABILITY

The V513 Module houses a VME RORA INTERRUPTER D08(o) type[1].This means that:

- it responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07;
- it removes its interrupt request when some on board registers are accessed by a VME MASTER (RORA: Release On Register Access).

5.2. INTERRUPT LEVEL

The interrupt level corresponds to the value stored in the Interrupt Level register <2..0>. the register is available at the VME address Base + % 02.

5.3. INTERRUPT STATUS/ID

The interrupt STATUS/ID is 8 bit wide, and it is contained in the Interrupt Vector register<7..0> (address Base + % 00).

5.4. INTERRUPT REQUEST RELEASE

The V513 INTERRUPTER removes its interrupt request in these cases:

- By accessing in write via VME the address Base + %40 (Clear VME interrupt));
- By accessing in write via VME the address Base + %42 (Module reset);
- By generating the VME signal SYSRES.

5.5. INTERRUPT SEQUENCE

If the VME interrupt level is different from 0:

{

- if Int Mask reg.<i>=1 and Input reg<i> becomes true or Strobe int =1 and the Strobe bit becomes true:

  {

  - It requests interrupt by driving an interrupt request line IRQ1..7 low according to the Interrupt Level register <2..0> value;

  - during the following acknowledge cycle it places on the VME data lines D00..D07 the STATUS/ID; it is the byte contained in the 8 LSB of the Interrupt vector register;

  }

- if the interrupt condition is removed (Int Mask reg=0 and Strobe int =0):

  {

  - if a VME MASTER accesses in write the address Base +% 40 (Clear VME interrupt) it releases its VME interrupt request line;

  }

}

6. REFERENCES

[1] VMEbus Specification Manual Revision C.1 October 1985

[2] G. Bianchetti et al., Specification for VMEbus CRATE Type V430, CERN-EP, January