Rev. 4 - Dec 13th, 2022

V4718/VX4718

VME to USB 3.0/Ethernet/Optical Link Bridge

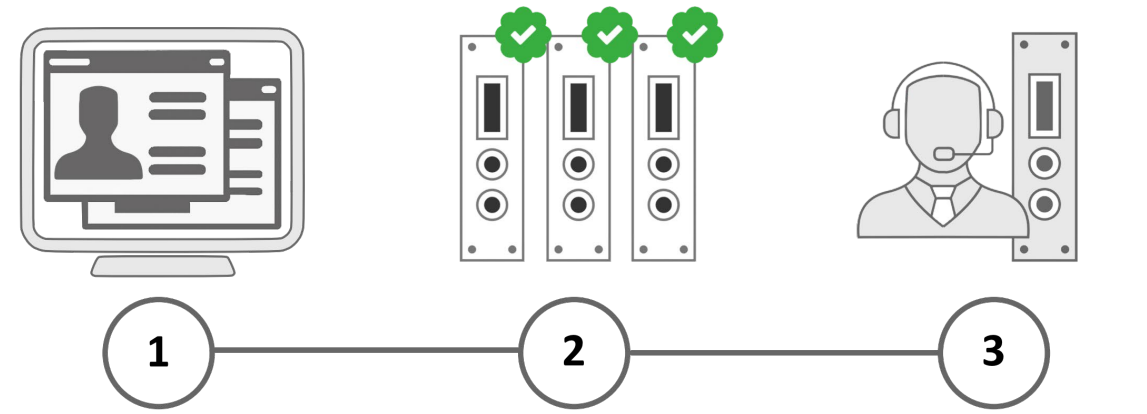
CAEN
Tools for Discovery

User Manual
UM8305

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual

This document contains the full hardware description of the V4718/VX4718 VME-to-USB-3.0/Ethernet/Optical Link Bridge.

Change Document Record

Date	Revision	Changes
August 30th, 2021	00	Initial release
October 18th, 2021	01	Updated Chap. **12** and **13**. Introduced the new CAEN Linux driver usage for the USB connection. Changed the string to connect by USB in the Web Interface.
January 3rd, 2022	02	Updated Sec. **First Access by USB**
August 30th, 2022	03	Corrected some bits in the register description
December 13th, 2022	04	Updated Chap. **14**. Add a note that specified that the USB connection is based on the IPv6 protocol.

Symbols, Abbreviated Terms and Notation

OS	Operative System
PCI	Protocol Control Information
SoC	System on Chip

Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide

[RD2] UM1934 - CAENComm User & Reference Manual

[RD3] UM1935 - CAENDigitizer User & Reference Manual

[RD4] UM7715 – CAENVMELib User & Reference Manual

[RD5] UM4413 - A2818 Technical Information Manual

[RD6] UM3121 - A3818 Technical Information Manual

[RD7] AN2472 - CONET1 to CONET2 migration

[RD8] DS7799 - A4818 USB 3.0 to CONET Adapter Datasheet

https://www.caen.it/support-services/documentation-area/

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

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Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

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1 Introduction

The V4718 is CAEN VME-to-USB 3.0/Ethernet/Optical Link Bridge implementing a VME master controlled by a PC via USB 3.0, Gigabit Ethernet and CONET Link (CAEN proprietary optical link protocol), including all the functions in a 1-unit wide VME 6U form factor. The V4718 is characterized by an enhanced data rate and extended interfacing capabilities, thanks to the on-board Zynq Ultrascale+ SoC module (including an ARM-based processor running Linux OS).

The Bridge is also available in the VX4718 version with VME64X mechanics (VME64X cycles not implemented). In the present document, the "V4718" term will be used to generally refer to both versions, unless otherwise specified.

The optical link connection between the V4718 and the host PC requires a CAEN optical controller (A3818 PCI Express or the A2818 PCI card) or the A4818 USB 3.0-to-CONET compact adapter, and an optical fiber cable (see **Tab. 1.1**). Multi-crate sessions can be easily performed thanks to the CONET Daisy chain capability: up to eight V4718 units can be controlled by a single link of an A2818/A3818/A4818 building a CONET Optical Network.

The V4718 is compliant with the USB 3.1 Gen1 speed protocol and can be connected to the USB port of the PC running Windows or Linux OS. The V4718 also have a 1 Gigabit Ethernet port allowing high data transfer rate.

The V4718 can perform all cycles foreseen by the VME64 standard except those intended for 3U boards. The Bridge can operate as VME System Controller (normally when plugged in the slot 1) acting as a Bus Arbiter in Multi-Master systems. The activity on the VME bus can be monitored in detail both locally (through an 88-LED DataWay Display) and remotely.

The front panel of the V4718 hosts 6 TTL/NIM programmable I/Os on LEMO connectors: four outputs (default assignment is: DSn, AS, DTK, BERR) and two inputs. The I/Os can be programmed via USB, Ethernet and Optical Link to implement functions like Timer, Counter, Pulse generator, I/O register, and others (see Chap. **8**).

The supported data transfer rate, with a CAEN slave readout in MBLT64 data transfer mode, is up to 60 MB/s by USB 3.0 and Ethernet and up to 80 MB/s by CONET2. Thanks to the 128KB memory buffer, the activity on the VME bus is not slowed down by the transfer rate on the USB port, on the Ethernet or on the CONET one, especially when several V4718 units share the same network.

The V4718 can be integrated into the most common Windows® and Linux® computers and middleware libraries are also provided. Moreover, the presence of an embedded Linux-based CPU gives to the user the chance of running custom software directly on-board.

The Web Interface of the V4718 allows the User to upgrade the firmware of the device, to set the Network parameters for the Ethernet connection, and to perform basic operations via the VME Bus (Read, Write, BLTRead, and BLTWrite).

THE SOFTWARE SUPPORT OF THE FRONT PANEL I/O PROGRAMMING IS FROM THE CAENVMELib LIBRARY REV.3.3 ON

Board Models	Description
V4718	V4718 – VME to USB 3.0/Ethernet/CONET Bridge
VX4718	VX4718 – VME to USB 3.0/Ethernet/CONET Bridge
Related Products	**Description**
A2818	A2818 – PCI Optical Link Controller
A3818A	A3818A – PCIe 1 Optical Link Controller
A3818B	A3818B – PCIe 2 Optical Link Controller
A3818C	A3818C – PCIe 4 Optical Link Controller
A4818	A4818 – USB 3.0 to CONET Adapter
Accessories	**Description**
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of models and related items

2 Block Diagram

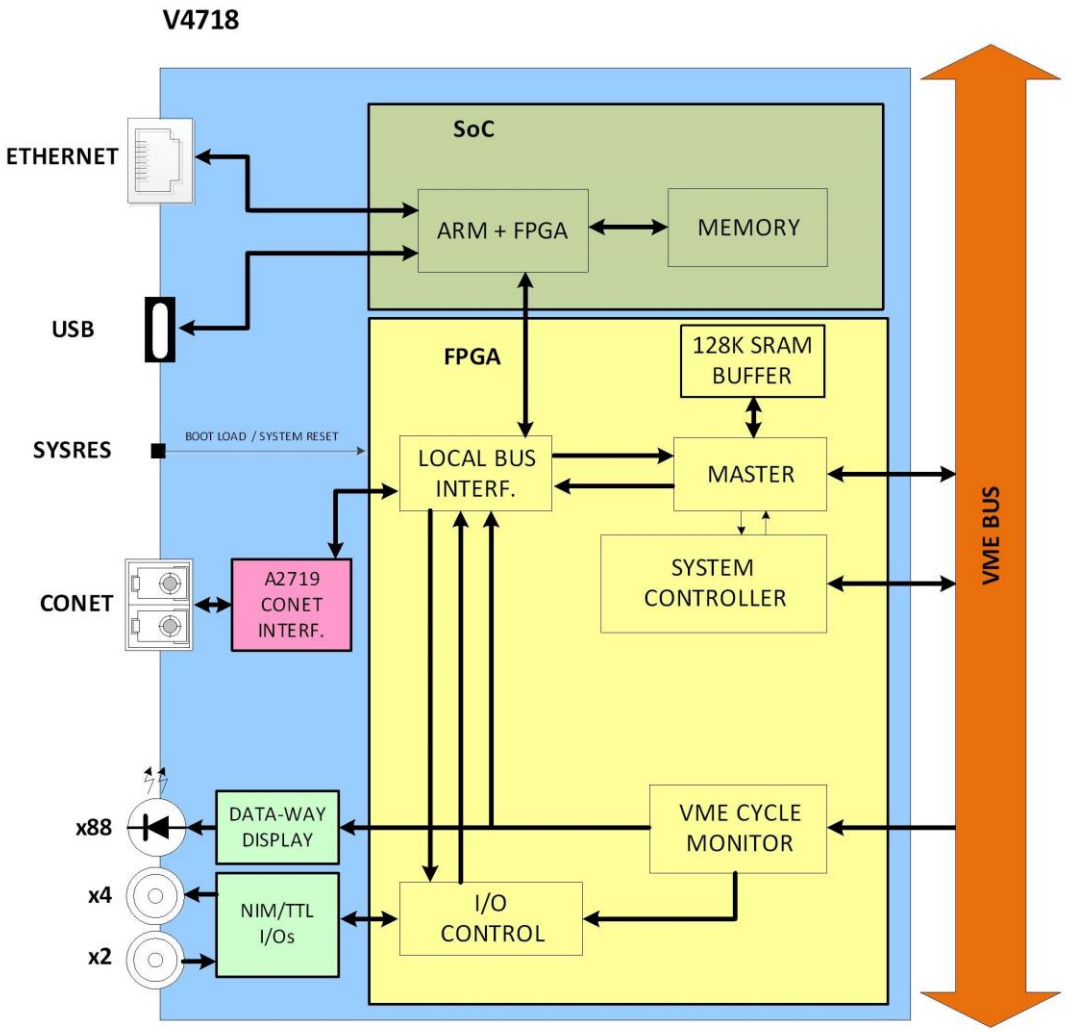

Fig. 2.1: Simplified block diagram

The FPGA represents the core of the module, implementing the CONET communication protocols, handling the LED display and I/O connectors on the front side and the VME Master on the back side. The USB 3.0 and Gigabit Ethernet communication protocols are managed by the embedded SoC which communicates with the FPGA local bus interface.

Inside the FPGA, a 128KB buffer permits temporary data storage during VME cycles: the VME data rate is therefore decoupled from the USB, Ethernet and optical link rate and may take place at full speed.

3 Technical Specifications

PHYSICAL	**Form Factor** 1-unit wide VME 6U	**Weight** 350g
PC INTERFACE	**USB** USB 3.0 Type-C socket **Ethernet** Gigabit Ethernet RJ45 connector	**Optical Link** CONET 2 (CAEN protocol) SFP+ connector
TRANSFER RATE	Maximum transfer rate with a CAEN slave readout in MBLT64: • Up to 80 MB/s via CONET2 • Up to 60 MB/s via USB 3.0 • Up to 60 MB/s via Ethernet	
ADDRESSING	A16, A24, A32, CR/CSR, LCK; ADO, ADOH cycles	
DATA CYCLES	D08, D16, D32 for R/W and RMW; D16, D32 for BLT, D64 for MBLT	
INTERRUPT CYCLES	D08, D16, D32, IACK	
INTERRUPTS TRANSFER AND MONITOR	**Optical Link** VME interrupts IRQ[7:1] passed directly from VME to the PCIe bus via optical link; the host system is notified asynchronously (polling not required) **Ethernet** VME interrupts are not directly passed to the PC; the host system has to poll IRQ[7:1] via Ethernet	**USB** VME interrupts are not directly passed to the PC; the host system has to poll IRQ[7:1] via USB
LED DISPLAY	Data bus, address bus, address modifier, interrupt request, control signals	
PANEL I/Os	**OUT[0:3]** 4 signal outputs SW programmable functions Single-ended NIM/TTL (R_t = 50 Ω) LEMO 00 female socket	**IN[0:1]** 2 signal inputs SW programmable functions Single-ended NIM/TTL (HW programmable) Z_{in} = 50 Ω or 1 kΩ hardware selectable LEMO 00 female socket
SOFTWARE	• Windows® and Linux® support • Drivers for the CONET communication link • Middleware C/C++ libraries • Web Interface for board control and firmware upgrade • Linux OS embedded on ARM processor	
POWER REQUIREMENTS	1.3 A @ +5V	0.050 A @ +12V 0.180 A @ -12V

Tab. 3.1: Specifications table

4 Packaging and Compliance

V4718/VX4718 are 1-unit wide 6U VME64/VME64X boards.

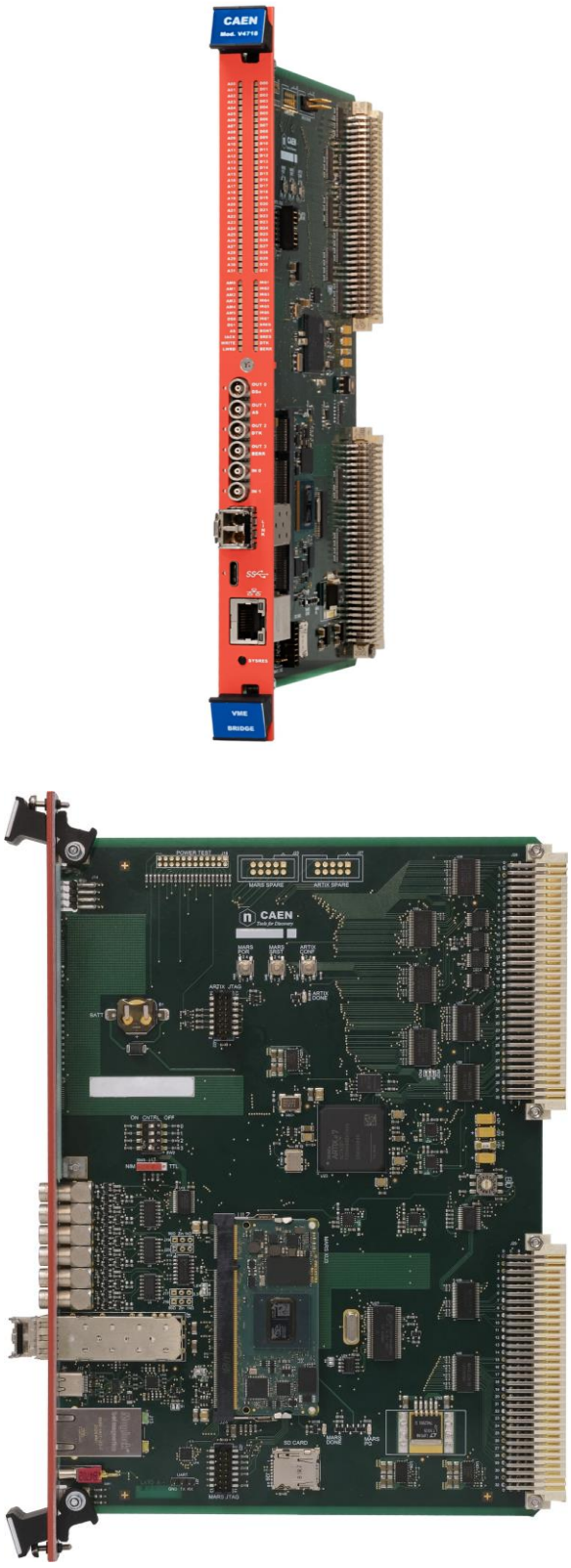

Fig. 4.1: Module views

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5 Panels Description

V4718 and VX4718 share the same panels arrangement.

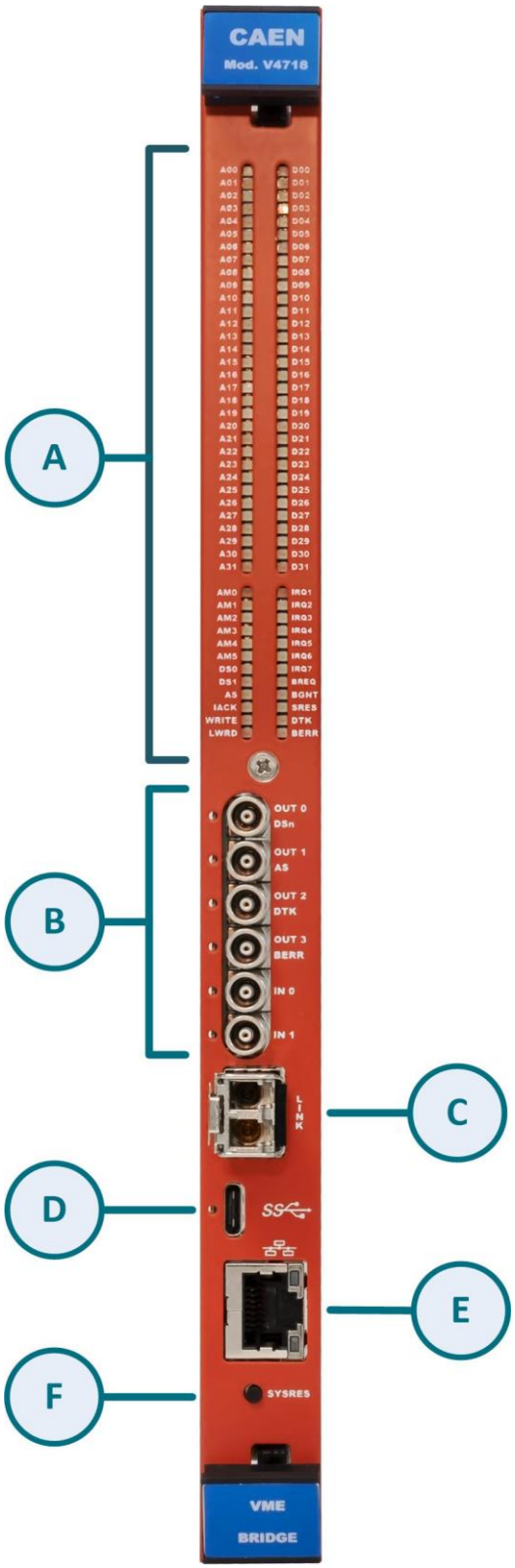


Fig. 5.1: Front panel

Front Panel

A

DATAWAY DISPLAY

FUNCTION

88-LED visual monitor of the activity on the VME bus (data bus, address bus, address modifier, interrupt request, control signals). See Chap. **7**.

B

DIGITAL INPUTS/OUTPUTS

FUNCTION

Four outputs and two inputs, NIM/TLL hardware selectable (see Chap. **8**). Inputs are internally terminated at 50 Ω or 1 kΩ by on-board jumper (see Chap. **6**); outputs require 50 Ω termination.

Default signals (see also Sec. **Internal Registers**)

- OUT 0 = DSn
- OUT 1 = AS
- OUT 2 = DTACK
- OUT 3 = BERR
- IN 0 = Scaler gate
- IN 1 = Scaler Input

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

INDICATORS

LEDs (GREEN): when on, indicate activity on the relevant I/O channel.

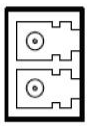
C

OPTICAL LINK PORT

FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides. Can support a maximum data rate of 80 MB/s.

PINOUT



TX (red wrap)

RX (black wrap)

MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8524P-2BNV (LC connectors).

Manufacturer: FINISAR.

INDICATORS

LEDs (GREEN/ORANGE)**:** GREEN LED indicates the network presence, while ORANGE LED signals the data transfer activity.

D

USB PORT

FUNCTION

USB connector for data readout and flow control. Compliant to USB 1.1, USB 2.0 and USB 3.0. Can support a maximum data rate of 60 MB/s.

MECHANICAL SPECS

Series: USB connectors.

Type: TYPE-C RECEPTACLE (632723300011).

Manufacturer: Wurth.

INDICATORS

LED (GREEN): indicates the USB communication is active.

E

ETHERNET PORT

FUNCTION

Ethernet connector (1000 base-T) for data readout and flow control. Can support a maximum transfer rate of 60 MB/s.

MECHANICAL SPECS

Series: RJ45 connectors.

Type: 0826-1A1T-23-F.

Manufacturer: Bel Fuse Inc.

INDICATORS

LEDs (GREEN/ORANGE)**:** GREEN LED indicates the network presence, while ORANGE LED signals the data transfer activity.

F

SYSTEM RESET BUTTON

FUNCTION

1) System Reset: hold the SYSRES button down until the SRES LED flashes on the dataway display (see Chap. **7**) to perform a system reset.
2) Boot load control: the button allows to alternatively enter the Backup mode or the Safe Mode, to possible recover from a partial or global FLASH issue (see Sec. **Troubleshooting**):
   - *No action*: power on the Bridge without any action on the SYSRES button. The Bridge will boot in Standard mode and the VME firmware copy (see Chap. **16**) stored in the Standard page of the FLASH is loaded on the FPGA (standard operating).
   - *Short pressure*: power on the crate holding the SYSRES button down and release the button as soon as the front panel I/O LEDs light on. The Bridge will boot in Backup mode and the VME firmware copy stored in the Backup page of the FLASH is loaded on the FPGA.
   - *Long pressure*: like short-pressure case but release the SYSRES button after the front panel I/O LEDs light off. The Bridge will boot in Safe Mode and the VME firmware copy stored in the Factory page of the FLASH is loaded on the FPGA.

Note: The System Reset Button does not allow to recover from partial or global FLASH issues related to the FPGA of the Zync Ultrascale+ SoC.

6 Internal Components

Switches

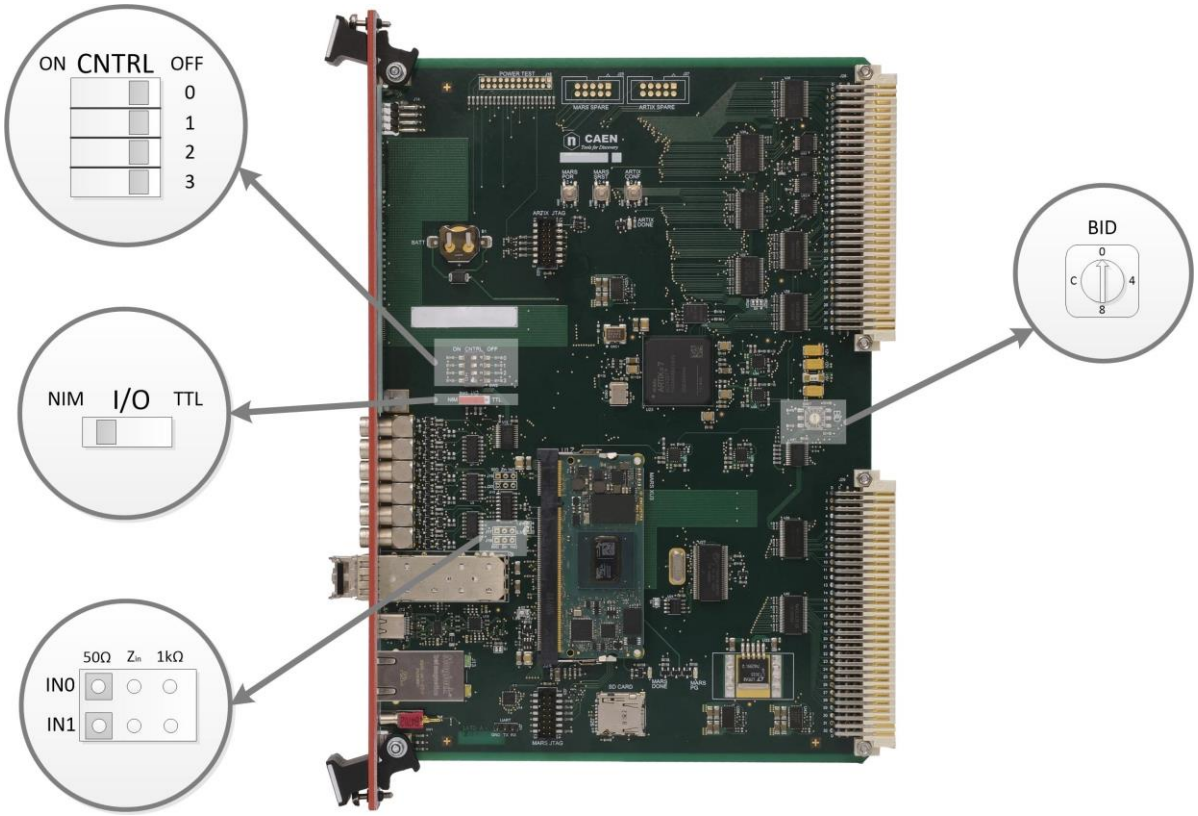


Fig. 6.1: Internal components

CTRL Dip Switches

Four selectors of VME functions; the status of each switch can be read also in the STATUS Register (see Sec. **Internal Registers**).

- **PROG[0]**: forces the System Controller to be enabled, regardless of the 1st Slot detection (ON: SYSTEM CONTROLLER enabled; OFF: don't care).
- **PROG[1]**: forces the System Controller to be disabled, regardless of the 1st Slot detection (ON: SYSTEM CONTROLLER disabled; OFF: don't care).
- **PROG[2]**: when this switch is ON, the master initiates the VME cycles without waiting for the Bus Grant from the arbiter; this setting must be used only for test purposes, since conflicts may occur when more VME masters are present (ON: requester bypassed; OFF: don't care).
- **PROG[3]**: *not used*.

NOTE: if PROG[0] is set to ON, then PROG[1] must be set to OFF and vice versa.

I/O Dip Switch

Common selector between NIM and TTL signals for the front panel I/Os (LEMO). The status of this switch can be read also in the STATUS Register (see Sec. **Internal Registers**).

INPUT Z_{in} Jumper

Selector of the input impedance for IN 0 and IN 1 front panel inputs: 50Ω default.

BID Rotary Switch

Board identifier (Board ID).

Product Identification Number (PID)

The PID is the unique CAEN product identification number composed of a prefix followed by an incremental number greater than 10000 (**Fig. 6.2**).

Fig. 6.2: PID label

The PID label is placed in the B-side of the V4718 board (**Fig. 6.3**).

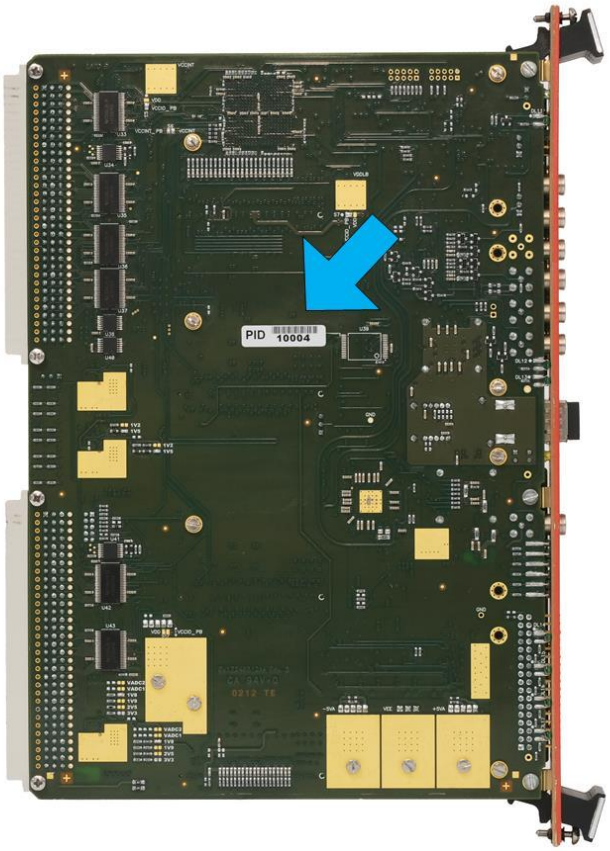


Fig. 6.3: PID location

7 VME Dataway Display

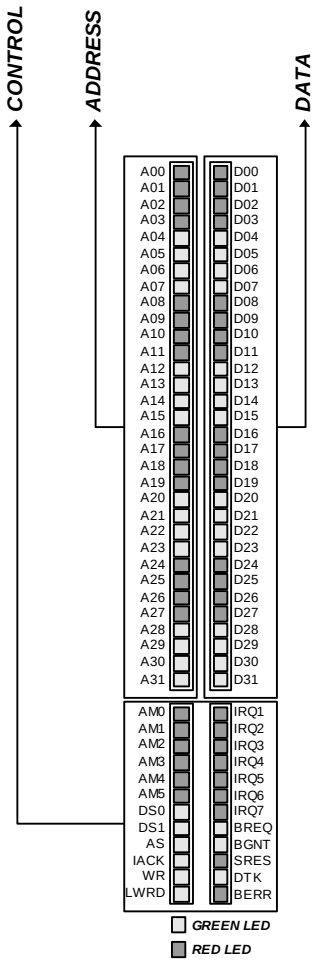


Fig. 7.1: Dataway display layout

The V4718 is provided with an 88-LED Dataway Display. The LEDs report the VME Bus status (address, data and control lines) related to the latest cycle.

NAME	FUNCTION
A[31:0] AM[5:0] IACK WRITE LWORD	These LEDs are frozen on the AS leading edge and remain stable until the next cycle
D[31:0]	These LEDs are frozen either on the DS leading edge during the write cycles or on the DTACK (or BERR) leading edge during the read cycles; the datum remains stable until the next cycle; in case of BLT cycles, the last read datum remains visible
DS0 DS1	These LEDs turn on as the signal is active during the cycle just executed; they remain stable until the next cycle
AS	This LED flashes on the AS leading edge; it is used for signaling a cycle execution
BGR	This LED flashes as any Bus Grant line (BG[3:0]) is active
BRQ	This LED flashes as any Bus Request line (BR[3:0]) is active
SRES	This LED flashes as the SYSRES is active (see Sec. **Front Panel**)
DTK	This LED turns on if the cycle just executed was terminated with a DTACK asserted by a slave; it remains on until the next cycle
BERR	This LED turns on if the cycle just executed was terminated with a BERR; it remains on until the next cycle

Tab. 7.1: Dataway display table

8 Programmable Inputs/Outputs

As described in Chap. **5**, the V4718 houses six software programmable GPIOs on the front panel: four outputs and two inputs. The signals can be either NIM or TTL, selectable by onboard dip switch (see Chap. **6**). Six green LEDs (one per connector) light up as the relevant signal is active.

The allowed programmable functions are the topic of this chapter, while the available registers are described in Sec. **Internal Registers**.

Timer & Pulse Generator

There are two modules implemented (Pulser A and Pulser B), which work independently. Each module produces a burst of N pulses (N can be infinite, then the pulses are continuously generated) upon a start signal which can be HW from a GPIO or SW from a register. The delay from the start signal, the pulser period T, and the pulse width W are programmable. The Pulser output can be directed to a GPIO. The stop, which can be HW from a GPIO or SW from a register, will interrupt the sequence and set to zero the outputs.

A schematic view of the main parameters is shown in **Fig. 8.1**.

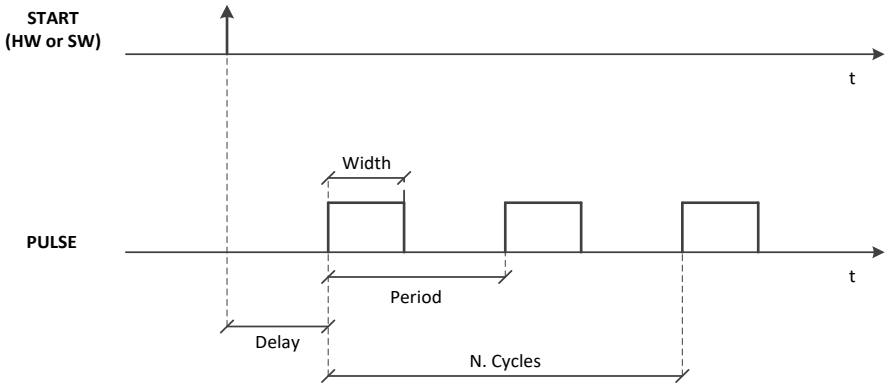


Fig. 8.1: Timer & Pulser Generator main parameters

By these modules, for example, it is possible to implement functions as:

- Clock Generator
- Burst Generator
- Monostable
- Gate and Delay Generator
- Set-Reset Flip-Flop

Scaler

There is a single scaler module implemented that can work in different modes. It allows counting a given signal in a previously set acquisition window that can be either a gate signal (Gate mode), or a preset time (D-Well Time mode), or a maximum number of hits (MaxHits mode). Whichever the mode, an analog signal can be generated on an output GPIO as soon as the end of the acquisition window is reached.

In Gate mode, the signal to count can be either an input GPIO (IN0, IN1), or a combination of the two input GPIO (coincidence signal: IN0 AND IN1; OR signal: IN0 OR IN1), or a VME signal (i.e. Data Strobe, Address Strobe, Data Acknowledge, Bus Error). The gate signal can be given by an input GPIO (IN0, IN1) or a software register. At the end of the gate, the number of counts is written in a register and an internal memory.

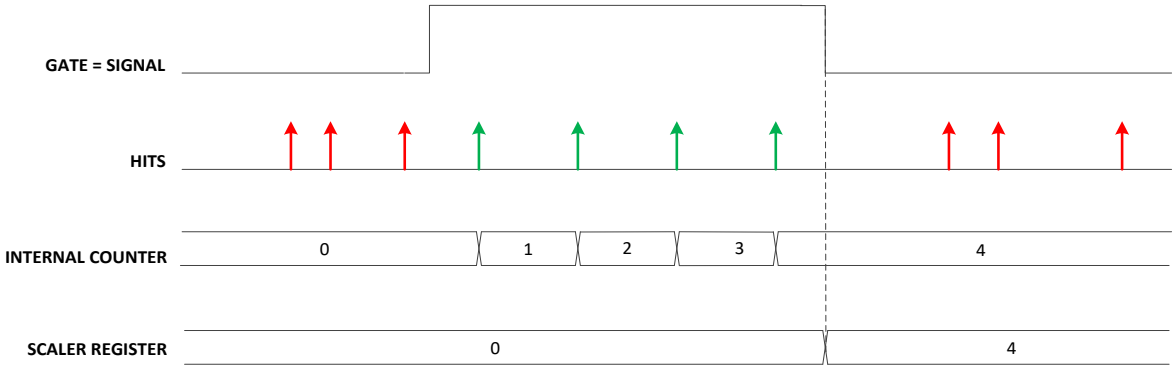


Fig. 8.2: Gate mode example. The gate is a given signal and only the hits within the gate (in green) are counted

In D-Well Time mode, an internal time gate (called D-Well Time), with a resolution of 1 ms, is applied to the scaler. At the end of the D-Well Time, the number of counts is written in a register and an internal memory.

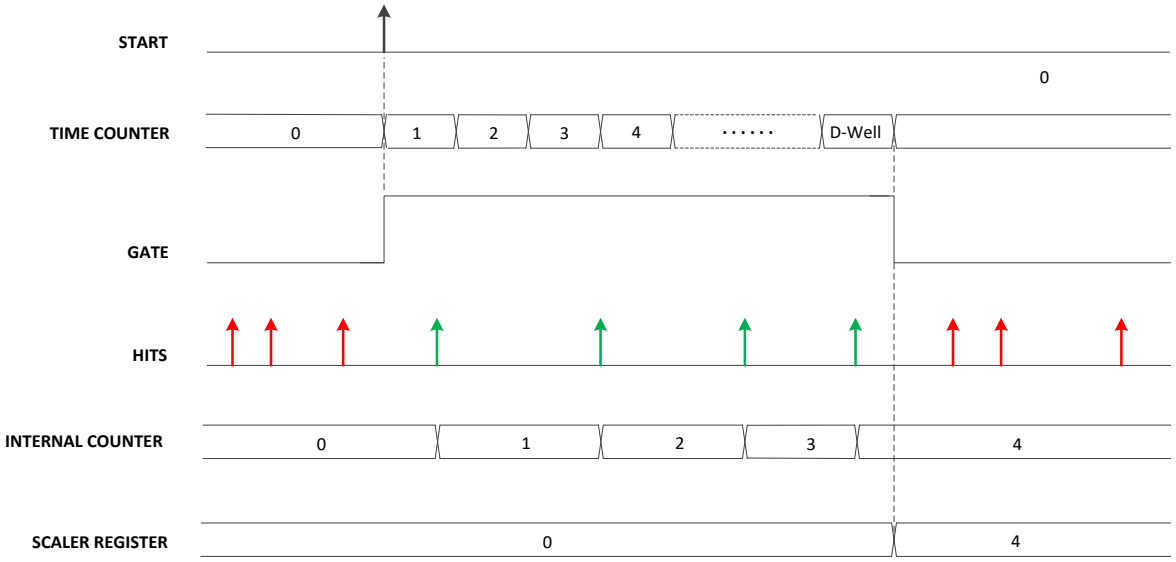


Fig. 8.3: D-Well mode example. Upon the start signal, the time counter starts counting the hits until the preset D-Well time is reached. Not counted hits are marked in red

In MaxHits mode, hits are counted until a hit number is reached.

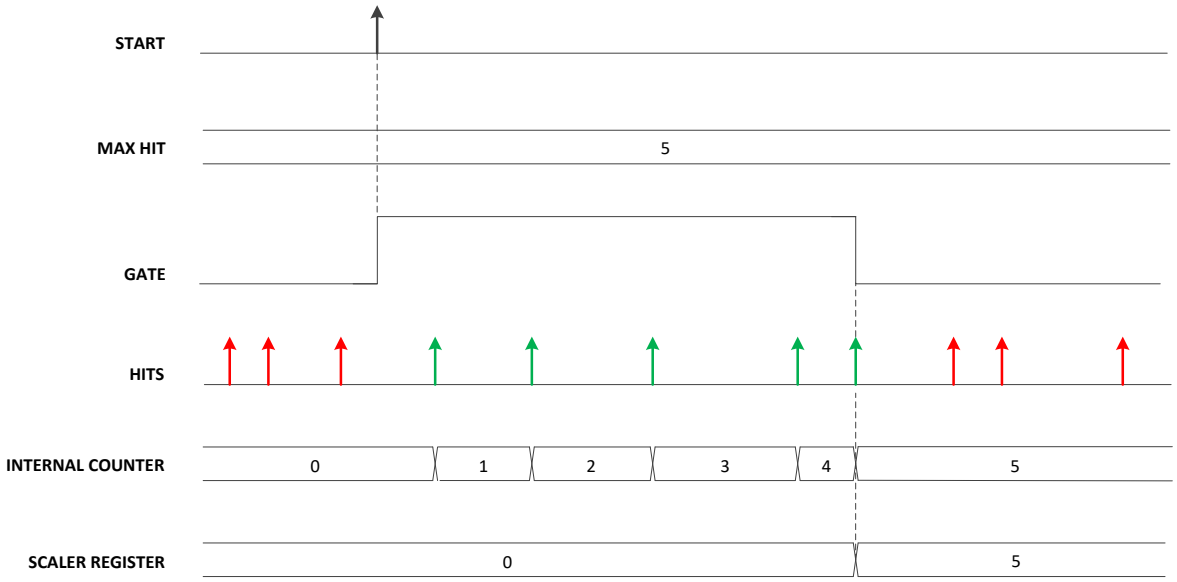


Fig. 8.4: MaxHit mode example. Upon the start signal, only a programmable maximum number of hits are counted

The Start Acquisition can be set either by an external signal (on level), or register, or front panel SYSRES button.

During the acquisition, the counter can be reset either by an external signal, or register, or front panel SYSRES button.

The run mode can be “Single Run” or “Continuous Run”. In the former case, as soon as the end of the first gate (in Gate mode), or the Dwell Time (in D-Well Time mode), or the number of hits (in MaxHits mode) is reached, the acquisition is stopped. In the latter case, the acquisition continues until the start signal is active.

Coincidence

This module makes the coincidence between two inputs. The coincidence signal is provided on the output when both the inputs are set to “1”. The output can be connected either to the input of other units or to an output GPIO.

Input/Output Register

The output signals can be programmed via an Output Register, while the input signals can be monitored via an Input Register.

9 Optical Link, USB and Ethernet Layout

The V4718 houses a USB3.0 compliant port with a maximum transfer rate of 60 MB/s, a Daisy chainable Optical Link (communication path which uses optical fibre cables as physical transmission line and CONET2 serial protocol) with a maximum transfer rate of 80 MB/s and an Ethernet port with a maximum transfer rate of 60 MB/s.

USB

A Point-to-point direct connection between the host PC and the V4718 Bridge is supported on any USB 3.0 compatible port.

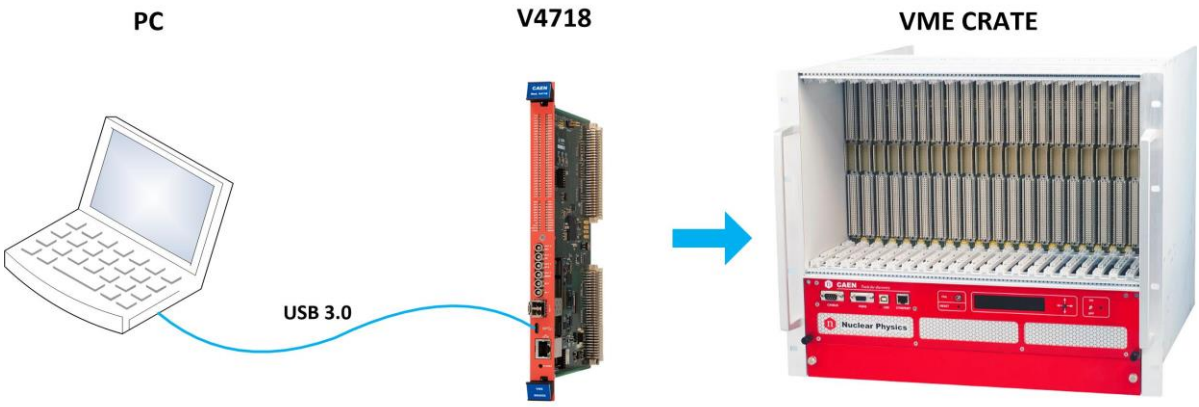


Fig. 9.1: Example of USB layout

Optical Link

Optical link connection between the V4718 Bridge and the host PC is based on CONET2 protocol and requires A2818 or A3818 CAEN Controller with a CONET2 firmware, or the A4818 Adapter board (see **Tab. 1.1**). Detailed information and documentation can be found on CAEN website in the relevant product web page **[RD4][RD6]**.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, Data Width, etc.); wrong parameter settings cause Bus Error.

Note: CONET2 is CAEN proprietary serial protocol developed to allow the optical link communication between the host PC, equipped with an A2818 or an A3818 Controller, and a CAEN CONET slave. CONET2 is 50% more efficient in the data transfer rate than the previous CONET1 version. The two protocol versions are not compliant to each other and before migrating from CONET1 to CONET2, it is recommended to read the instructions provided by CAEN in the dedicated Application Note **[RD7]**.

CONET1 IS SUPPORTED ONLY BY THE A2818 PCI CONTROLLER!

IT IS SO STRICTLY REQUIRED TU UPGRADE THE A2818 WITH A CONET2 FIRMWARE BEFORE COMMUNICATING WITH THE V4718!

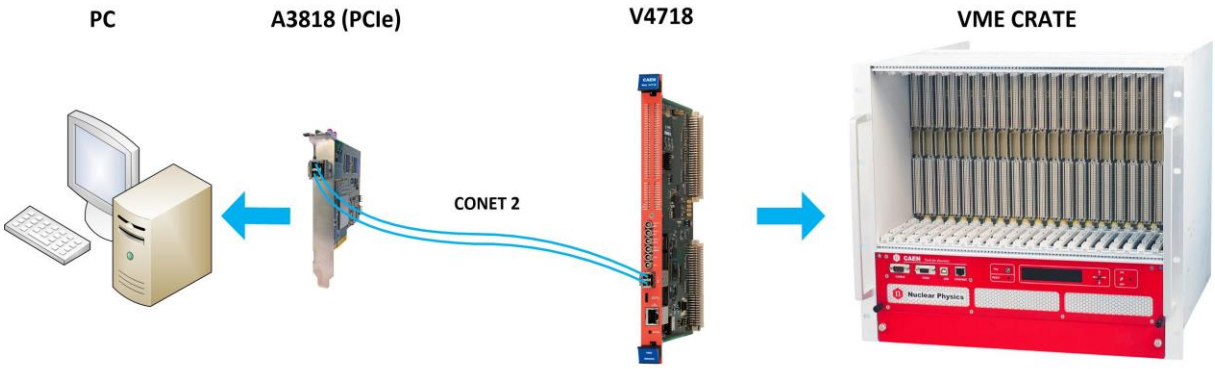


Fig. 9.2: Example of Optical Link setup through A3818 (or A2818)

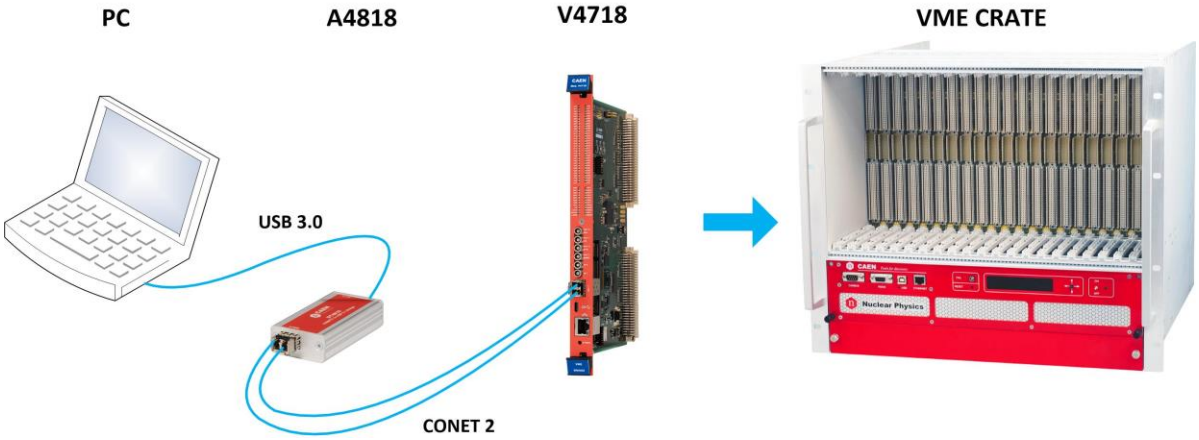


Fig. 9.3: Example of Optical Link setup through A4818

The CAEN Optical Link features Daisy chain capabilities: up to eight CONET slave nodes can be connected in Daisy chain to the link of the A2818 or A4818, and to each link of a multi-link A3818 version. The A3818C (4-links) can support up to 32 CONET slave nodes in Daisy chain. For this purpose, various types of cables are available (see **Tab. 9.1**).

Cable	Length	Connector
X-30	30 m	1 LC Duplex + 2 LC Simplex
X-20	20 m	1 LC Duplex + 2 LC Simplex
X-5	5 m	1 LC Duplex + 2 LC Simplex
I-40	40 m	2 LC Simplex
I-30	30 m	2 LC Simplex
I-20	20 m	2 LC Simplex
I-5	5 m	2 LC Simplex
I-3	30 cm	2 LC Simplex

Tab. 9.1: CONET cables specifications

If the network is composed by one A2818, A3818 or A4818, and only one V4718, then it is suggested to use X-type cables: such cables have a duplex connector on the A2818/A3818/A4818 side and two simplex connectors on the crate side; the simplex connector with the black wrap is for the RX line and the one with the red wrap is for the TX. If more than one V4718 are present, the best solution is to use the X-type cable for connecting the A2818/A3818/A4818 with the first and the last module, and the I-type for connecting intermediate modules. An example is given in **Fig. 9.4**.

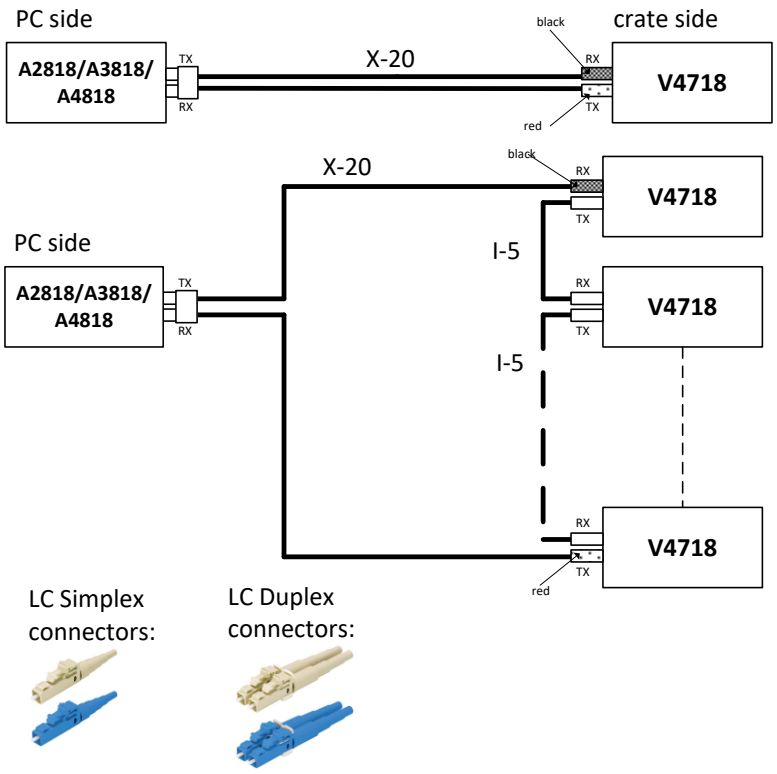


Fig. 9.4: Example of optical network

Ethernet

The V4718 Ethernet connector allows the user either to perform a point-to-point connection between the host PC and the module (see **Fig. 9.5**) or to connect to it via a LAN network.

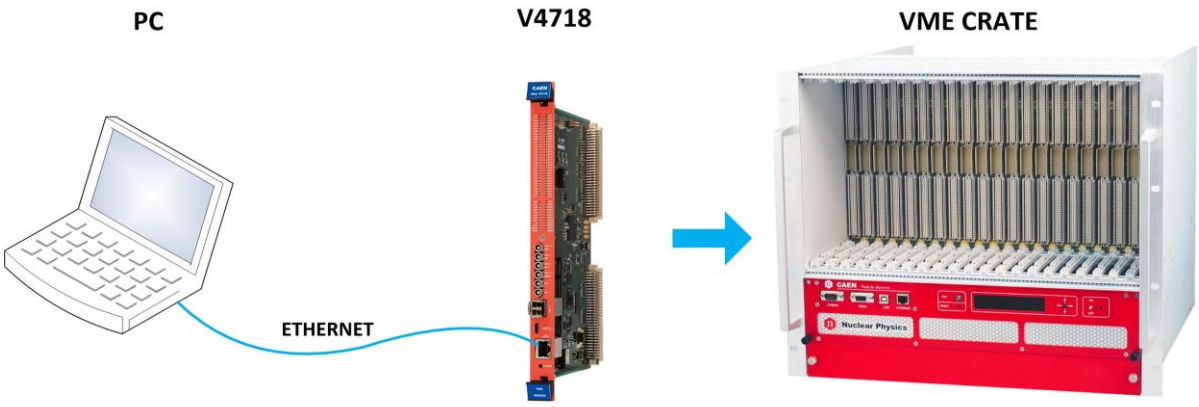


Fig. 9.5: Example of point-to-point Ethernet connection

10 VME Interface

The V4718 provides all the addressing and data transfer modes documented in the VME64 specification (except A64 and those intended to improve 3U applications, like A40 and MD32). The V4718 is also compatible with all VME bus modules compliant to pre-VME64 specifications. As VME bus master, the V4718 supports Read-Modify-Write (RMW), and Address-Only-with-Handshake (ADOH) but does not accept RETRY* as a termination from the VME bus slave. The ADOH cycle is used to implement the VME bus Lock command allowing the PC Host to lock VME bus resources.

VME Bus Requester

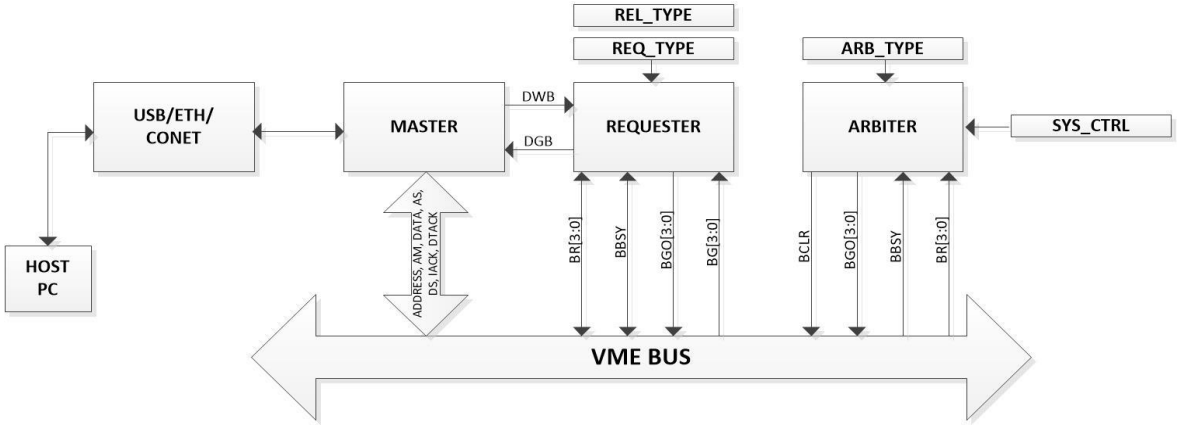


Fig. 10.1: Internal arbitration for VME bus request

When the V4718 operates as VME bus Requester, the functional sequence is as follows:

- The USB/ETH/CONET sends a VME bus access request.
- The Master asserts DWB (Device Want Bus) and waits for DGB (Device Grant Bus).
- The Requester requests the bus to the Arbiter, via VME (whether the Arbiter is the V4718 itself or not); when the Arbiter has granted the bus, the Requester asserts DGB and BBSY (on the bus).
- The Master performs the VME cycle, then releases DWB.
- If REL_TYPE is RWD (Release When Done), then the Requester releases BBSY.

Fair and Demand Request Modes

The V4718 produces requests on all VME bus request levels: BR3*, BR2*, BR1*, and BR0*. The default setting is for level 3 VME bus request. The request level is a global programming option set through the Bus Request field in the Control register (see Sec. **Internal Registers**).

The programmed request level is used by the VME bus Master Interface regardless of the channel currently accessing the VME bus Master Interface.

The Requester may be programmed for either Fair or Demand mode. The request mode is a global programming option set through the Requester Type bit in the Control register.

In Fair mode, the V4718 does not request the VME bus until there are no other VME bus requests pending at its programmed level. This mode ensures that every requester on an equal level has access to the bus.

In Demand mode, the requester asserts its bus request regardless of the state of the BRn* line. By requesting the bus frequently, requesters far down the daisy chain may be prevented from ever obtaining bus ownership. This is referred to as “starving” those requesters. Note that, to achieve fairness, all bus requesters in a VME bus system must be set to Fair mode.

VME Bus Release

The Requester can be configured as either RWD (Release When Done) or ROR (release on request) using the Release Type bit in the Control register (see Sec. **Internal Registers**). The default setting is for RWD: the bus is released as soon as the VME access is terminated; in case of BLT/MBLT cycles, the access is terminated either when the N required bytes are transferred (although the cycle is divided into several blocks according to the VME boundaries) or when BERR* is asserted. ROR means the master releases BBSY* only if a bus request is pending from another VME bus master and once the channel that is the current owner of the VME bus Master Interface is done. Ownership of the bus may be assumed by another channel without re-arbitration on the bus if there are no pending requests on any level on the VME bus.

Addressing Capabilities

The V4718 generates A16, A24, A32, CR/CSR and LCK address phases on the VME bus. Address Modifiers of any kind (supervisor/non-privileged and program/data) are also programmed through USB, Ethernet or CONET: the V4718 does not handle the AM; the HOST PC passes them via USB or Ethernet as VME cycle parameters. The AM broadcasting depends on the PC drivers.

The master generates ADdress-Only-with-Handshake (ADOH) cycles in support of lock commands for A16, A24, and A32 spaces.

Supported addressing:

A16, A24, A32, CR/CSR	for R/W, RMW, ADO and ADOH
A16, A24, A32	for BLT
A16, A24, A32	for MBLT
ADO	Address Only
ADOH	Address Only with Handshake

Data Transfer Capabilities

The V4718 supports the following cycles:

Cycle Type

R/W	Single Read/Write
RMW	Read Modify Write
BLT	Block Transfer
MBLT	Multiplexed Block Transfer

Data sizing

D08(EO), D16, D32	for R/W, RMW, BLT
D64	for MBLT

- BLT/MBLT cycles may be performed with either address increment or with fixed address (FIFO mode)
- BLT/MBLT cycles are split at hardware level when the boundary (BLT = Nx256 bytes; MBLT = Nx2 Kbytes) is met: AS is released and then re-asserted, the VME bus is not re-arbitered. The boundaries are neglected in FIFO operating mode.
- Non-aligned accesses are not supported

It is then possible to perform data cycles (single and BLT) with hardware byte swapping. The “Swapped” cycles are called: D16_swapped, D32_swapped and D64_swapped. Such cycles will return “swapped” data, in the following way:

D16_swapped: Byte0 ↔ Byte1, Byte1 ↔ Byte0

D32_swapped: Byte0 ↔ Byte3, Byte1 ↔ Byte2, Byte2 ↔ Byte1, Byte3 ↔ Byte0

D32_swapped: Byte0 ↔ Byte7, Byte1 ↔ Byte6, Byte2 ↔ Byte5, Byte3 ↔ Byte4, Byte4 ↔ Byte3, Byte5 ↔ Byte2, Byte6 ↔ Byte1, Byte7 ↔ Byte0

Interrupt Capabilities

USB Link

The USB link does not allow transferring an interrupt to the PC, so the communication between the PC and the V4718 is always started by the PC. The VME interrupts are activated by reading the IRQ lines status from the PC and, if one line is active, then a IACK cycle can be executed.

The V4718 supports the following IACK cycles:

IACK: D08, D16, D32

Ethernet Link

The Ethernet link does not allow transferring an interrupt to the PC, so the communication between the PC and the V4718 is always started by the PC. The VME interrupts are activated by reading the IRQ lines status from the PC and, if one line is active, then a IACK cycle can be executed.

The V4718 supports the following IACK cycles:

IACK: D08, D16, D32

Optical Link

The VME Bus interrupts are transferred to the PCI/PCIe BUS through the CONET. The interrupt latency (i.e. the interval between the interrupt appearance on the VME bus and the time the interrupt is activated on the PCI bus) is always shorter than 5 µs.

The V4718 supports the following IACK cycles:

IACK: D08, D16, D32

The VME Bus Interrupts can be individually masked for each V4718 in the chain.

The CAENVMLib library (see Chap. **15**) makes available specific functions like the first-to-be-used *IRQEnable()* which enables the generation of PCI bus interrupts following VME bus interrupts, and the *IRQWait()* that must be then called to wait for the interrupt. When the *IRQWait()* returns, the VME bus interrupts are disabled, so an IACK can be performed in order to obtain the vector and, for RORA interrupts, the access to the interrupter must be performed in order to stop the interrupt generation. If it is necessary to receive other VME bus interrupts, the IRQEnable must be called again. Find detailed description in the library documentation **[RD4]**.

Cycle Terminations

The V4718 accepts BERR* or DTACK* as cycle terminations. BERR* is handled as cycle termination whether it is produced by the V4718 itself or by another board. The Status word broadcasted as the cycle is acknowledged, informs the HOST PC about the cycle termination type (BERR* or DTACK*).

VME Bus First Slot Detector

The First Slot Detector module samples BG3IN* immediately after reset to determine whether the V4718 resides in slot 1. The VME bus specification requires the BG[3:0]* lines to be driven high during reset. This means that, if a board is preceded by another board in the VME bus system, it will always sample BG3IN* high after reset. BG3IN* can only be sampled low after reset by the first board in the crate (there is no preceding board to drive BG3IN* high). If BG3IN* is sampled at logic low immediately after reset (due to the master internal pull-down), then the V4718 is in slot 1 and becomes SYSTEM CONTROLLER; otherwise, the SYSTEM CONTROLLER module is disabled. This mechanism may be overridden via dip switch setting: the SYSTEM CONTROLLER bit is “forced” to one by setting to ON PROG_0, and is “forced” to zero by setting to ON PROG_1; note that such switches must always be in “opposite” positions (see Chap. **6**).

System Controller Functions

When located in Slot 1 of the VME crate, the V4718 assumes the role of SYSTEM CONTROLLER and sets the SYSTEM CONTROLLER status bit in the STATUS register (see Sec. **Internal Registers**). In accordance with the VME64 specification, as SYSTEM CONTROLLER the V4718 provides:

- a system clock driver

- an arbitration module
- an IACK Daisy Chain Driver (DCD)
- a bus timer

System Clock Driver

The V4718 provides a 16MHz SYSCLK signal when configured as SYSTEM CONTROLLER.

Arbitration Module

When the V4718 is SYSTEM CONTROLLER, the Arbitration Module is enabled. The Arbitration Module supports the following arbitration modes:

- Priority Based (PRI),
- Round Robin Select (RRS) (default setting).

These modes can be set in the CONTROL register (see Sec. **Internal Registers**).

In the Priority Based Mode (PRI), the order of priority is BR[3], BR[2], BR[1], and BR[0] as defined by the VME64 specification. The Arbitration Module issues a Bus Grant (BGO[3:0]) to the highest requesting level. If a Bus Request of higher priority than the current bus owner becomes asserted, the Arbitration Module asserts BCLR until the owner releases the bus (BBSY is negated).

Round Robin Select mode (RRS) arbitrates all levels in a round robin mode, repeatedly scanning from levels 3 to 0. Only one grant is issued per level and one owner is never forced from the bus in favour of another requester (BCLR is never asserted). Since only one grant is issued per level on each round robin cycle, several scans will be required to service a queue of requests at one level.

Bus Timer

A programmable bus timer allows users to select a VME bus time-out period. The time-out period is configurable as 50 µs or 400 µs through the Bus Timeout bit in the Control register (see Sec. **Internal Registers**). The VME bus Timer module asserts BERR if a VME bus transaction times out (indicated by one of the VME bus data strobes remaining asserted beyond the time-out period).

IACK Daisy Chain Driver

The V4718 can operate as IACK Daisy Chain Driver: it drives low the IACKOUT line of the first slot, thus starting the chain propagation, as soon as it detects an Interrupt Acknowledge cycle by an Interrupt Handler (that could be the V4718 itself).

VME64X Cycles

The VME64X cycles are not implemented in this board.

Internal Registers

NAME	ADDRESS	TYPE	Nbit	FUNCTION
STATUS	0x00	read	16	Status register
CONTROL	0x01	read/write	16	VME control register
FIRMWARE_REVISION	0x02	read	16	FW revision register
IRQ_STATUS	0x05	read	16	IRQ status register
IRQ_MASK	0x06	read/write	16	IRQ mask register
IO_LEVEL	0x07	Read/write	16	I/O level set register
IO_POLARITY	0x08	read/write	16	I/O polarity register
OUT_2_0_MUX_SET	0x09	read/write	16	OUT[2:0] Multiplexer set register
OUT3_MUX_SET	0x0A	read/write	16	OUT[3], IN[1:0] Multiplexer set register
IO_STATUS_READ	0x0B	read/write	16	I/O status read register
IO_STATUS_SET	0x0C	read/write	16	I/O status set register
IO_COINC	0x0D	read/write	16	I/O coincidence mask register
PULSE_A_SETUP	0x10	read/write	16	Pulser A source register
PULSE_A_START	0x11	read/write	16	Pulser A start register
PULSE_A_CLEAR_(STOP)	0x12	read/write	16	Pulser A clear (stop) register
PULSE_A_NCYCLE	0x13	read/write	16	Pulser A n cycles register
PULSE_A_WIDTH	0x14	read/write	16	Pulser A width register
PULSE_A_DELAY	0x15	read/write	16	Pulser A dealy register
PULSE_A_PERIOD	0x16	read/write	16	Pulser A period register
PULSE_B_SETUP	0x17	read/write	16	Pulser B source register
PULSE_B_START	0x18	read/write	16	Pulser B start register
PULSE_B_CLEAR_(STOP)	0x19	read/write	16	Pulser B clear (stop) register
PULSE_B_NCYCLE	0x1A	read/write	16	Pulser B n cycles register
PULSE_B_WIDTH	0x1B	read/write	16	Pulser B width register
PULSE_B_DELAY	0x1C	read/write	16	Pulser B dealy register
PULSE_B_PERIOD	0x1D	read/write	16	Pulser B period register
DISPLAY_ADDRESS_LOW	0x20	read	16	Display AD[15:0] register
DISPLAY_ADDRESS_HIGH	0x21	read	16	Display AD[31:16] register
DISPLAY_DATA_LOW	0x22	read	16	Display DT[15:0] register
DISPLAY_DATA_HIGH	0x23	read	16	Display DT[31:16] register
SCALER_SETUP	0x2D	read/write	16	Scaler source register
SCALER_MAXHITS	0x2E	read/write	16	Scaler end counter register
SCALER_DWELL_TIME	0x2F	read/write	16	Scaler dwell time register
SCALER_SW_SETTING	0x30	read/write	16	Scaler gate and reset signal register
SCALER_INST_OUT	0x31	read/write	16	Scaler instantaneous out register
SCALER_FIFO_OUT	0x32	read/write	16	*To be implemented*

Fig. 10.2: Register map

STATUS Register

This register contains information on the status of the module.

Bit	Description
[0]	SYSTEM RESET: 0 = Inactive 1 = Active
[1]	SYSTEM CONTROL: 0 = Disabled 1 = Enable
[3:2]	*reserved*
[4]	DTACK: 1 = Last cycle terminated with DTACK 0 = Any other case
[5]	BERR: 1 = Last cycle terminated with BERR 0 = Any other case
[7:6]	*reserved*
[8]	Status of Dip Switch 0: 0 = Switch set to OFF 1 = Switch set to ON
[9]	Status of Dip Switch 1: 0 = Switch set to OFF 1 = Switch set to ON
[10]	Status of Dip Switch 2: 0 = Switch set to OFF 1 = Switch set to ON
[11]	Status of Dip Switch 3: 0 = Switch set to OFF 1 = Switch set to ON
[12]	*reserved*
[13]	NIM/TTL STATUS: 0 =NIM 1 = TTL
[15:14]	*reserved*

CONTROL Register

This register allows performing some general settings of the module.

Bit	Description
[0]	*reserved*
[1]	ARBITER TYPE: 0 = Fixed Priority 1= Round Robin
[2]	REQUESTER TYPE: 0 = Fair 1 = Demand
[3]	RELEASE TYPE: 0 = Release When Done (RWD) 1 = Release On Request (ROR)
[5:4]	BUS REQUEST LEVEL
[6]	INTERRUPT REQUEST
[7]	SYSTEM RESET (SysRes)
[8]	BUS TIMEOUT: 0 = 50 µs 1 = 400 µs
[9]	ADDRESS INCREMENT DURING BLT: 0 = enabled 1 = disabled (FIFO mode)
[10]	SINGLE CYCLE SEQUENCE
[15:11]	*reserved*

FIRMWARE REVISION Register

This register contains the firmware revision number coded over 16 bits as X.Y.

Bit	Description
[7:0]	MINOR REVISION NUMBER (Y)
[15:8]	MAJOR REVISION NUMBER (X)

IRQ STATUS Register

This register monitors the IRQ lines status

Bit	Description
[0]	IRQ LINE 1: 0 = inactive 1 = active
[1]	IRQ LINE 2: 0 = inactive 1 = active
[2]	IRQ LINE 3: 0 = inactive 1 = active
[3]	IRQ LINE 4: 0 = inactive 1 = active
[4]	IRQ LINE 5: 0 = inactive 1 = active
[5]	IRQ LINE 6: 0 = inactive 1 = active
[6]	IRQ LINE 7: 0 = inactive 1 = active
[15:7]	*reserved*

IRQ MASK Register

This register set the IRQ mask.

Bit	Description
[6:0]	IRQ LINE [6:0]
[15:7]	*reserved*

I/O LEVEL SET Register

This register allows setting the TTL/NIM level for the I/O front panel signals.

Bit	Description
[1:0]	*reserved*
[2]	*reserved* (must be 1)
[3]	*reserved* (must be 1)
[4]	*reserved* (must be 0)
[5]	*reserved* (must be 0)
[6]	HW/SW Level selection: 0 = selection is HW (see Chap. **6**) 1 = selection is SW (*default*)
[7]	Level selection: 0 = NIM (*default*) 1 = TTL
[15:8]	*reserved*

I/O POLARITY Register

This register allows inverting the polarity of the front panel I/O signals. Direct means the original polarity, which could be active low or active high. Inverting an active-low I/O then means to set it active high, and vice versa.

Bit	Description
[0]	OUT0 polarity: 0 = direct (*default*) 1 = inverted
[1]	OUT1 polarity: 0 = direct (*default*) 1 = inverted
[2]	OUT2 polarity: 0 = direct (*default*) 1 = inverted
[3]	OUT3 polarity: 0 = direct (*default*) 1 = inverted
[4]	IN0 polarity: 0 = direct (*default*) 1 = inverted
[5]	IN1 polarity: 0 = direct (*default*) 1 = inverted
[15:6]	*reserved*

OUT [2:0] MULTIPLEXER SET Register

This register allows to set the function for OUT0, OUT1, and OUT2 front panel I/Os.

Bit	Description
[3:0]	OUT0 function: 0000 = Data Strobe signal (*default*) 0001 = Address Strobe signal 0010 = Data Acknowledge signal 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT0 is set at 0)
[7:4]	OUT1 function: 0000 = Data Strobe signal 0001 = Address Strobe signal (*default*) 0010 = Data Acknowledge signal 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT1 is set at 0)
[11:8]	OUT2 function: 0000 = Data Strobe signal 0001 = Address Strobe signal 0010 = Data Acknowledge signal (*default*) 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT2 is set at 0)
[15:12]	*reserved*

OUT [3] MULTIPLEXER Register

This register allows to set the function for OUT2, OUT3, IN0 and IN1 front panel I/Os.

Bit	Description
[3:0]	OUT3 function: 0000 = Data Strobe signal 0001 = Address Strobe signal 0010 = Data Acknowledge signal 0011 = Bus Error signal (*default*) 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved*
[15:4]	*reserved*

I/O STATUS READ Register

This register allows to read the instantaneous status of the front panel I/Os.

Bit	Description
[0]	OUT0 Status
[1]	OUT1 Status
[2]	OUT2 Status
[3]	OUT3 Status
[4]	IN0 Status
[5]	IN1 Status
[15:6]	*reserved*

I/O STATUS SET Register

This register allows setting the value of the front panel I/Os. To be effective, the I/O function must be set correctly first (see Sec. **OUT [2:0] MULTIPLEXER SET Register** and Sec. **OUT [3] MULTIPLEXER Register**).

Bit	Description
[0]	OUT0 Set
[1]	OUT1 Set
[2]	OUT2 Set
[3]	OUT3 Set
[15:4]	*reserved*

I/O COINCIDENCE Register

This register allows setting the mask for the coincidence mode.

Bit	Description
[1:0]	*reserved*
[2]	IN0: 0 = not in coincidence 1 = participates in coincidence
[3]	IN1 0 = not in coincidence 1 = participates in coincidence
[15:4]	*reserved*

PULSE A SETUP Register

This register allows setting the Pulser A sources for the start signal and the clear signal. The clear signal allows restarting the pulse train from the beginning.

Bit	Description
[0]	Start signal source: 0 = SW (*default*) 1 = HW
[1]	Clear signal source: 0 = SW (*default*) 1 = HW
[15:2]	*reserved*

PULSE A START Register

This register allows to physically start Pulser A.

Bit	Description
[0]	SW start signal: 0 = not issued (*default*) 1 = issued
[3:1]	HW start signal: 010 = IN 0 011 = IN 1 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE A CLEAR Register

This register allows to physically clear Pulser A. This means resetting the counter and waiting for a 0 to 1 transition of the start command. In the case of start source by SW, it must be set at 0 and then to 1 again.

Bit	Description
[0]	SW clear signal 0 = not issued (*default*) 1 = issued
[3:1]	HW clear sources: 010 = IN 0 (set as input) 011 = IN 1 (set as input) 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE A N CYCLE Register

This register allows to set the number of pulses and the resolution for Pulser A. Default register value is 0x0000.

Bit	Description
[14:0]	Number of pulses
[15]	Clock resolution: 0 = 25 ns 1 = 25 µs

PULSE A WIDTH Register

This register allows setting the width of the pulse for Pulser A with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse width

PULSE A DELAY Register

This register allows setting the delay of the pulse for Pulser A with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse delay

PULSE A PERIOD Register

This register allows setting the period of the pulse with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse period

PULSE B SETUP Register

This register allows setting the Pulser B sources for the start signal and the clear signal. The clear signal allows restarting the pulse train from the beginning.

Bit	Description
[0]	Start signal source: 0 = SW (*default*) 1 = HW
[1]	Clear signal source: 0 = SW (*default*) 1 = HW
[15:2]	*reserved*

PULSE B START Register

This register allows to physically start Pulser B.

Bit	Description
[0]	SW start signal: 0 = not issued 1 = issued (*default*)
[3:1]	HW start signal: 010 = IN 0 011 = IN 1 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE B CLEAR Register

This register allows to physically clear Pulser B. This means resetting the counter and waiting for a 0 to 1 transition of the start command. In the case of start source by SW, it must be set at 0 and then to 1 again.

Bit	Description
[0]	SW clear signal is issued
[3:1]	HW clear sources: 010 = IN 0 (set as input) 011 = IN 1 (set as input) 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE B N CYCLE Register

This register allows setting the number of pulses and the resolution for Pulser B.

Bit	Description
[14:0]	Number of pulses
[15]	Clock resolution: 0 = 25 ns 1 = 25 µs

PULSE B WIDTH Register

This register allows setting the width of the pulse for Pulser B with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse width value

PULSE B DELAY Register

This register allows setting the delay of the pulse for Pulser B with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse delay value

PULSE B PERIOD Register

This register allows setting the period of the pulse with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse period value

SCALER SETUP Register

This register allows to set the source of the Scaler input, gate and reset.

Bit	Description
[3:0]	Scaler Input-Source setting: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal 0011 = IN 1 signal (*default*) 0100 = VME Data Strobe signal 0101 = VME Address Strobe 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1010 = Coincidence signal of IN0/IN1 1011 = N0 OR IN1 signal Others = *reserved*
[7:4]	Scaler Gate-Source Setting: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal (*default*) 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*
[11:8]	Scaler Counter Reset: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** (*default*) 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*

[15:12]	Scaler Start Source: 0000 = reserved (do not use) 0001 = reserved (do not use) 0010 = IN 0 signal 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** (*default*) 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*

SCALER MAXHITS Register

This register allows setting the number of events to stop the counter. As soon as the number of hits reaches the register value, the Scaler is stopped.

Bit	Description
[15:0]	Max hits value

SCALER DWELL TIME Register

This register allows setting the time interval (in ms) to store hits. As soon as the time interval is reached, the counter is sent out to the Instantaneous out and the FIFO out, and a new counter is set to store new data.

Bit	Description
[15:0]	D-Well time value

SCALER SW SETTINGS Register

This register manages to set the gate, reset Scaler signals, and start the acquisition.

Bit	Description
[0]	Scaler SW gate (gate is opened by software)
[1]	Scaler SW reset (counters are reset by software)
[2]	Scaler SW Start (the start count is given by software)
[3]	Run mode: 0 = Continuous run (*default*) 1 = Single run

SCALER INSTANTANEOUS OUT Register

This register allows reading only the last output data of the Scaler (if not read, values are lost).

Bit	Description
[15:0]	Scaler data

SCALER FIFO OUT Register

This register allows reading the output data of the Scaler stored in a time interval (if not read, values are lost).

Bit	Description
[15:0]	Scaler data

DISPLAY ADDRESS LOW Register

This register monitors the Address bit[15:0] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_AD[15:0]

DISPLAY ADDRESS HIGH Register

This register monitors the Address bit[31:16] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_AD[31:16]

DISPLAY DATA LOW Register

This register monitors the Data bit[15:0] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_DATA[15:0]

DISPLAY DATA HIGH Register

This register monitors the Data bit[31:16] section of the front panel LED Display.

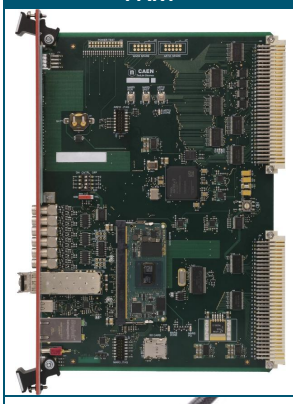
Bit	Description
[15:0]	DISP_DATA[31:16]

11 Hardware Installation

Delivered Kit

The V4718 is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects. When receiving the unit, the user is strictly recommended to inspect for any damage which may have occurred during transportation. Particularly, inspect for exterior damages like broken knobs or connectors, and check that the panels are not scratched or cracked. All packing material should be held on until the inspection has been completed. If a damage is detected, the user must fill a claim with the carrier immediately and notify CAEN.

Before installing the unit, make sure to read thoroughly the safety rules and installation requirements (see Sec**. Safety Notices**), then place the package content onto your bench. The content should consist in the parts listed below.

PART	DESCRIPTION
	V4718 module
	Hi-Speed Type A-to-Type C USB 3.1 Cable assembly - 1.8 m
	Ethernet Cable A-MCSSP60020-R Assmann – 2 m
	User Manual

Safety Notices

- The V4718 fits into 6U VME crates.
- The VX4718 fits into 6U VME64X compliant crates.
- Use only crates with forced cooling air flow.
- Turn off the crate before board insertion/removal.
- Remove all cables connected to the front panel before board insertion/removal.

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

THIS BRIDGE DOES NOT SUPPORT LIVE INSERTION (HOT SWAP)!
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before to operate with CAEN equipment.

Power-on

To power on the board, perform the following steps:

1. Insert the V4718 into the crate
2. Power up the crate

Power-on Status

At power-on, the V4718 module visualize the VME firmware release (see Chap. **16**) and immediately after, the dataway display LEDs turn on. Then, the LEDs of the dataway display start to turn on/off sequentially as to signal the loading of the board (see **Fig. 11.1**). As soon as the loading process is completed, the LEDs of the dataway display turn off and the board is ready to be used.

Fig. 11.1: LED Status after V4718 power-on.

After power-on, the module is in the following status:

- Registers are set to their default configuration.
- All dataway display LEDs are turned off.

12 Hardware Detection

It is required to install the driver provided by CAEN only in the case of USB connection in Linux OS (see Sec. **USB Configuration**). When performing a TDLink connection to the module, the driver of the optical link controller/adapter used needs to be installed (see Sec. **Optical Link Configuration**).

The V4718 is factory provided with the default IP address **192.168.1.254** that can be changed by the User in the dedicated Web Interface (Chap. **13**). For the USB connection, the hostname is fixed, and it is **V4718-USB-PID**, where PID is the unique product identifying number described in Sec. **Product Identification Number (PID)**.

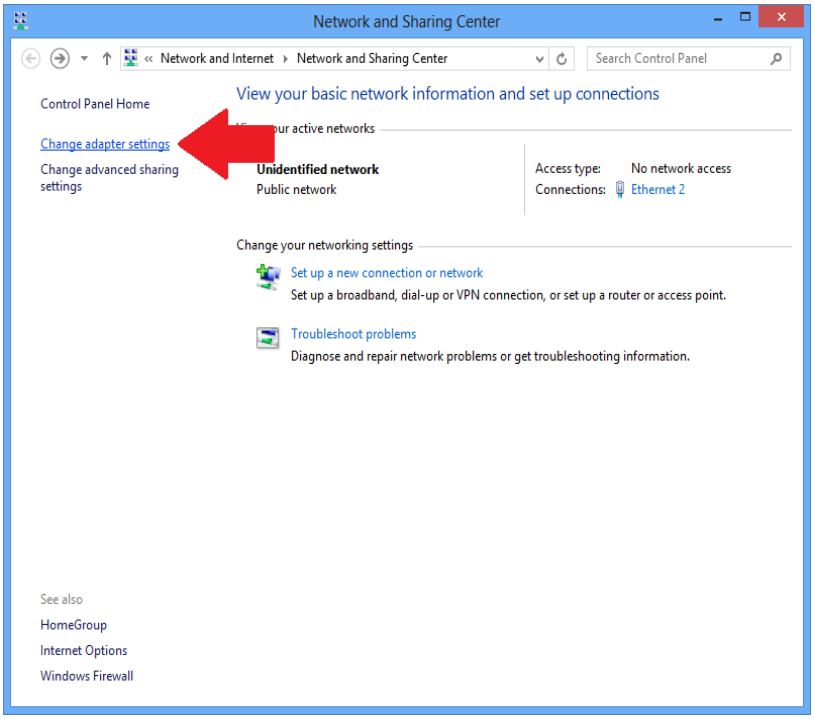
Ethernet Configuration

It is possible to connect the Ethernet interface of the V4718 through a server or through a point-to-point connection with a PC. In the latter case, the connection can be done using either a crossed cable, a switch, or a computer with an Ethernet port. The Ethernet connection to the V4718 Bridge does not require the installation of any CAEN driver, both in Windows and Linux OS.

Windows OS

Point-to-point configuration instructions are described below for Windows® 10 OS.

1.



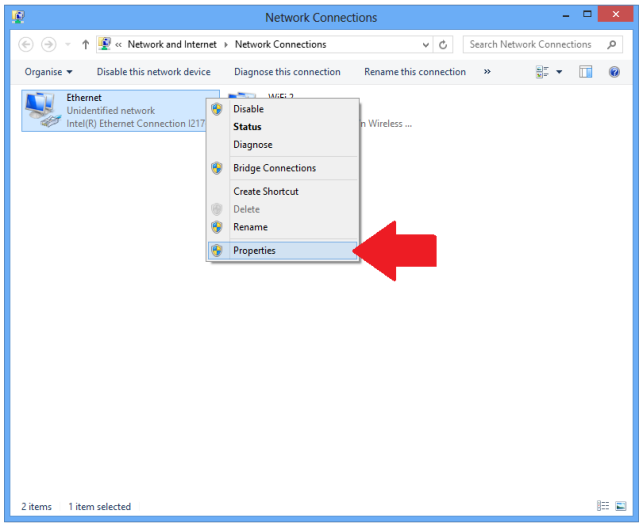
- Power on the V4718 and the PC.
- Connect the Ethernet cable between the V4718 and the host PC.
- Open the Windows path:

  Control Panel -> Network and Internet -> Network and Sharing Center

- Click on “Change adapter settings” as in the figure above.

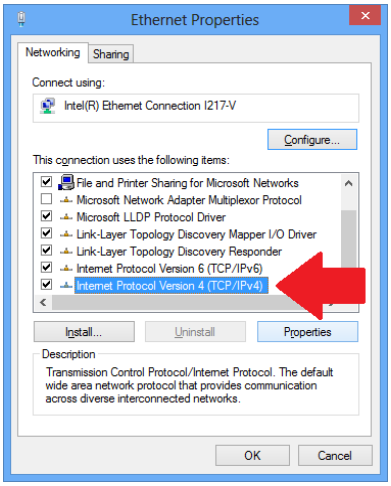
2.

- Right-click on the Ethernet icon and select ”Properties”.



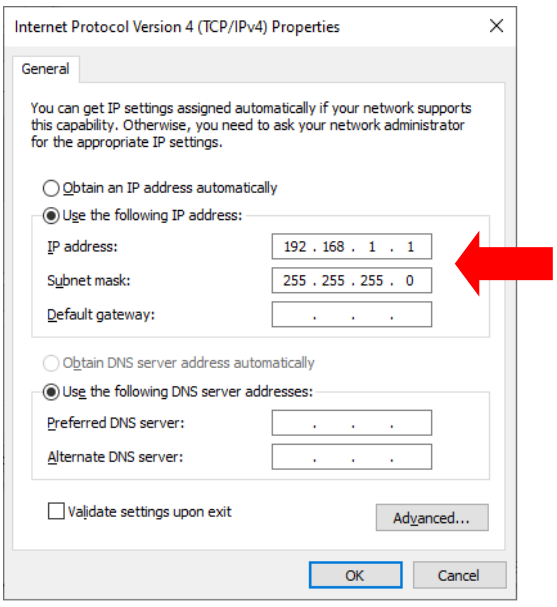
3.

- Click on ”Internet Protocol Version (TPC/IPv4)” and select ”Properties”.

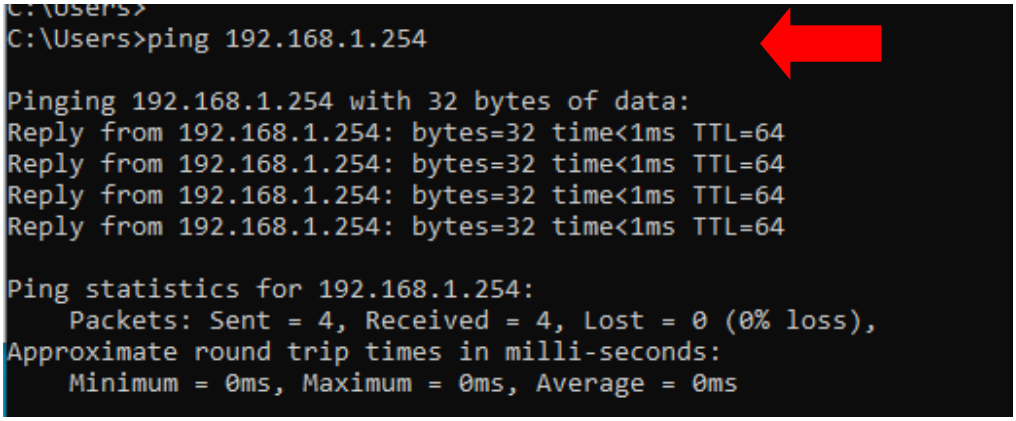


4.

- Type in the IP address, where the network part is fixed and specifies the unique number assigned to the User network, while the host part must be customized to identify the machine in your network. The figure on the right shows an IP address example.
- Type in the subnet mask as 255.255.255.0.



5.



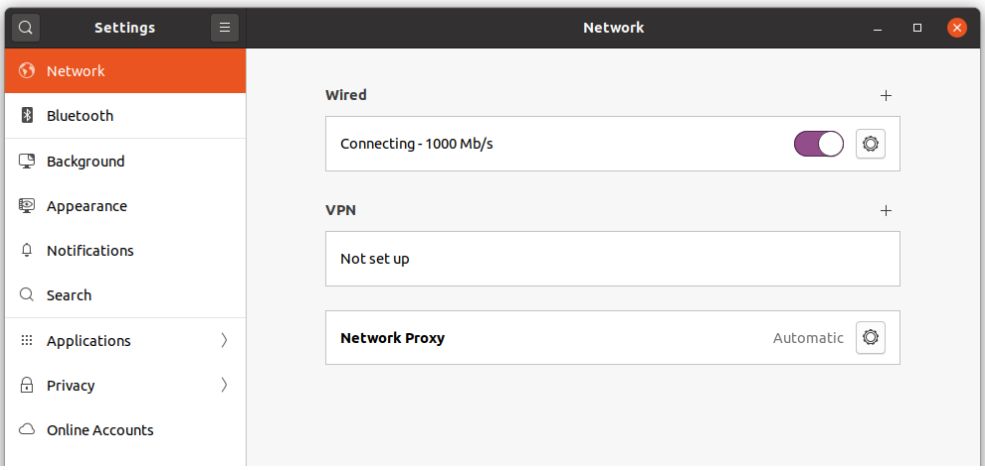
- The User can test if the communication between the PC and the V4718 is correctly established by performing a ping to the board
- In order to do so, the User should open the "Command Prompt" window and type in the string: *ping IP address*

  where the IP address is that of the V4718 board (192.168.1.254 by default)
- If the connection is correctly established, the output messages should be similar to that displayed in the figure above. In all other cases, the user is kindly suggested to re-check all the passages described in this section.

Linux OS

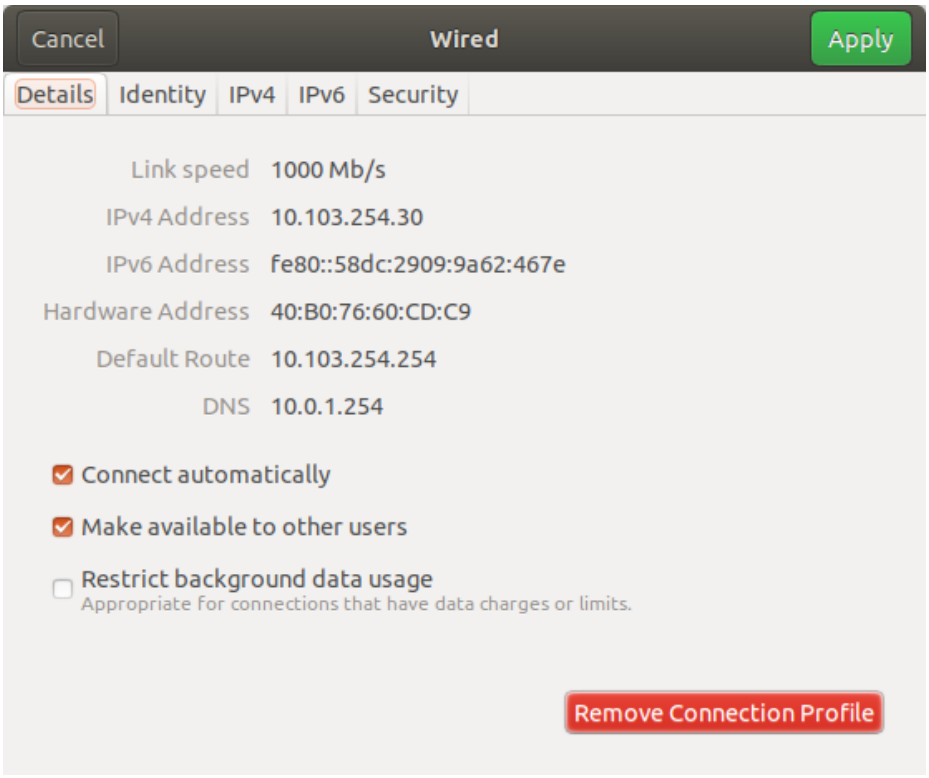
A similar procedure is foreseen with a point-to-point configuration on Linux®, as described below for Ubuntu Linux rel. 20.04.

1.



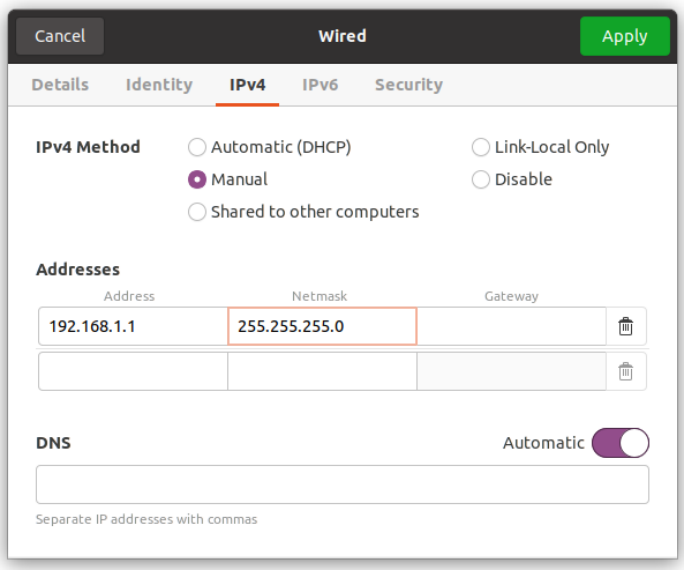
- Power on the V4718 and the PC.
- Connect the Ethernet cable between the V4718 and the host PC.
- Click on the top-right Network icon or access the Network activity. The window that will open should be similar to the one shown in the figure above.

2.



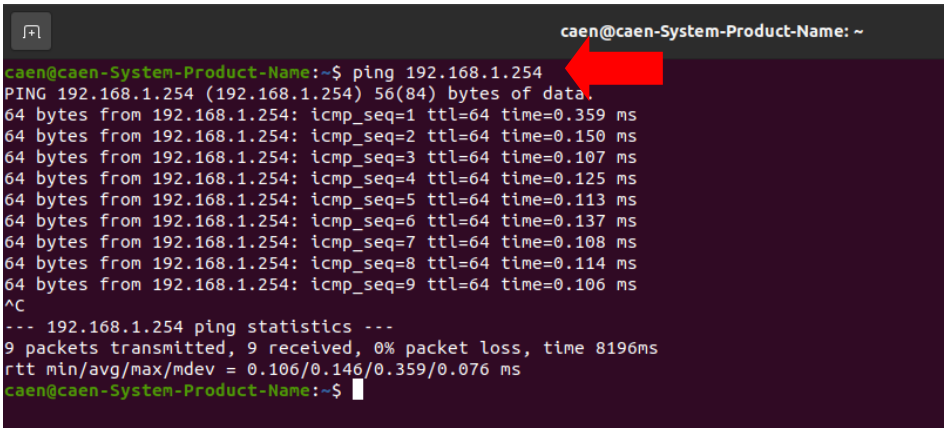
- Click on the gear in the Wired section of the Network window in order to modify the wired connection settings. The window that will open should be similar to the one shown above. Alternatively, the User can create a New Profile of wired connection by clicking on the + button in the Wired section of the Network window.

3.



- Select the IPv4 tab, put a thick on Manual for the IPv4 Method section, configure the IP Address and Netmask, and then press Apply. The figure above shows a typical setting example for a point-to-point connection between the V4718 (with a default IP address of 192.168.1.254) and the PC.

4.



- The User can test if the communication between the PC and the V4718 is correctly established by performing a ping to the board
- In order to do so, open the terminal and type in the string: *ping IP address*

  where the IP address is the one of the V4718 board (192.168.1.254 by default)
- If the connection is correctly established, the output messages should be similar to that displayed in the figure above. In the other case, the user is kindly suggested to re-check all the passages described in this section.

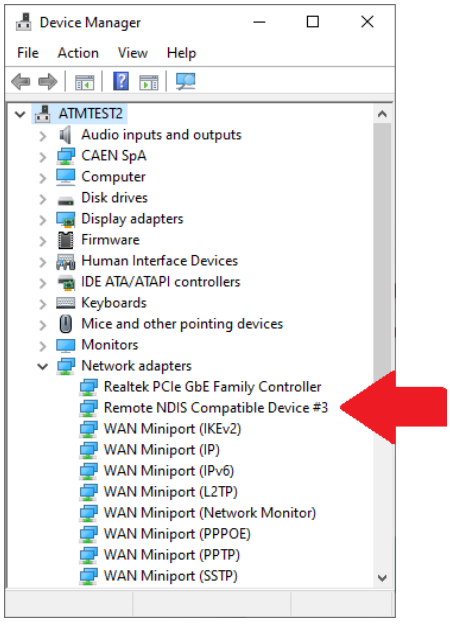
USB Configuration

The USB 3.0 interface of the V4718 is based on the IPv6 protocol. Make sure to enable the protocol required to communicate with the device.

Windows OS

1.

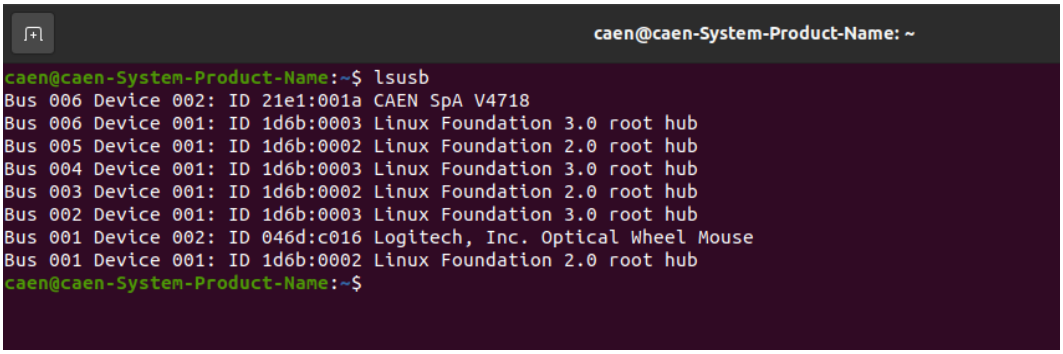
- Power on the digitizer and the PC.
- Connect the USB cable between the Digitizer and the host PC.
- The new hardware will be automatically detected as “Remote NDIS Compatible Device #n” in Windows Device Manager under Network Adapters (see figure on the right).



Linux OS

1.

- Download the driver for Linux from the V4718 web page and unpack it.
- Execute: *sudo ./install.sh* (as reported in the README file). The script file will properly configure the system to manage the USB connection by the hostname (see Sec. **First Access by USB**).



- Connect the USB cable between the Digitizer and the host PC.
- Power on the digitizer and the PC.
- The new hardware will be automatically detected.
- Issue the *lsusb* command to list the connected USB peripherals and look for the “CAEN SpA V4718” voice in the results (see figure above).

Optical Link Configuration

Once connected the Bridge to the host PC by the Optical Link fibre and powered on both, the user needs to install the required drivers for the optical controller/adapter and Operating System.

Optical Link Drivers

The optical link CONET protocol is managed by the A2818 (PCI), A3818 (PCIe) controllers and by the A4818 USB 3.0 to CONET adapter. The driver installation packages are downloadable for free on CAEN website in the controller and adapter pages (**login required**).

For the installation of the A2818 and A3818 Optical Link driver, refer to the controller User Manual **[RD5][RD6]**. For the installation of the A4818 adapter, refer to the adapter Datasheet **[RD8]**.

13 Web Interface

The V4718 is provided with a web interface that manages a set of service operations both via USB and Ethernet interface.

The web interface is organized into different pages and is schematically represented in **Fig. 13.1**.

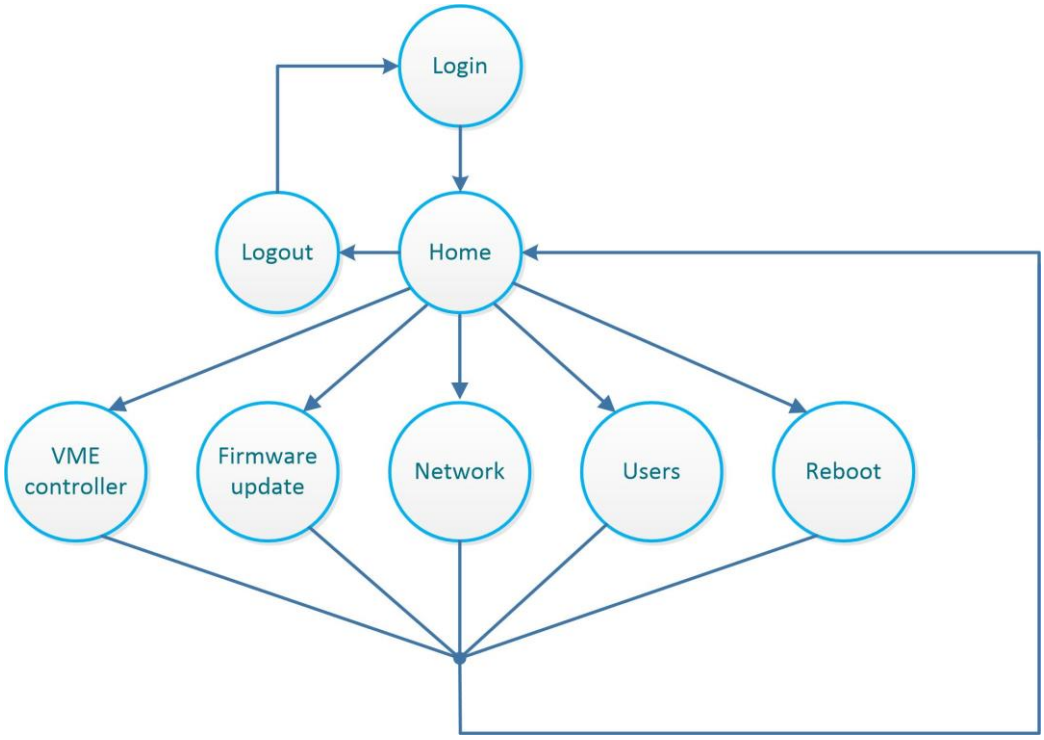


Fig. 13.1: Flow Diagram of the Web Interface

First Access by USB

To perform the first access by USB, open your browser and digit:

http://V4718-USB-PID.local

where the PID is the number reported on your V4718 module (see Sec. **Product Identification Number (PID)**).

NOTE THAT there might be some Linux distributions that are not able to automatically retrieve the Bridge USB name (V4718-USB-{PIDNUMBER}). In this case, the web browser returns an error when trying to access the Bridge using its USB name. This issue can be resolved by connecting the Bridge to a PC USB port (there must be only one CAEN device at a time connected!) and then executing the regPID.sh script file (./regPID.sh) that is included in the Linux driver packet of the Bridge (see Chap. **12**). The connected Bridge will be so registered in the PC. In presence of multiple Bridges, the same procedure must be repeated for each device.

First Access by Ethernet

To perform the first access by Ethernet, open your browser and digit:

http://192.168.1.254

where 192.168.1.254 is the factory IP address of the board (see Sec. **Ethernet Configuration**).

Note: since the User can modify the factory IP address (see Sec. **Network**), it is strongly suggested to check the IP address of the V4718 by the web interface connecting via USB link first.

Login

Log in to the Web Interface by using the default credentials:

Username = *admin*

Password = *admin*

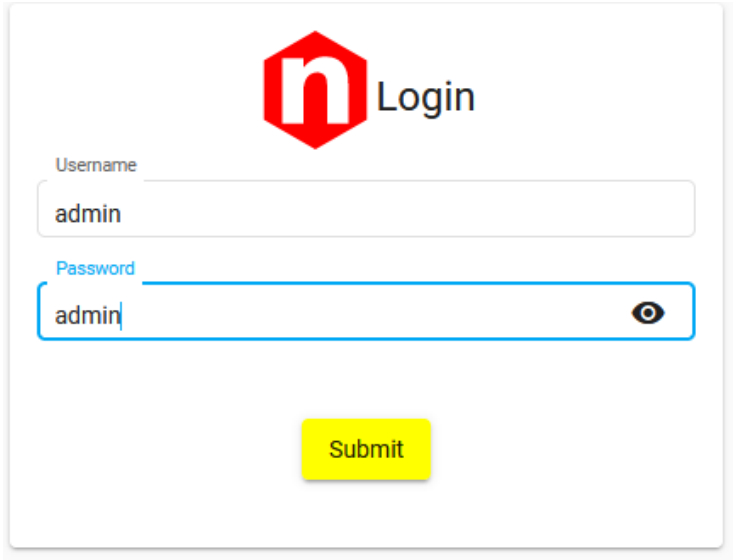


Fig. 13.2: Login window

VME controller

Once the User has entered the Web Interface, the VME controller page is immediately opened (see **Fig. 13.3**).

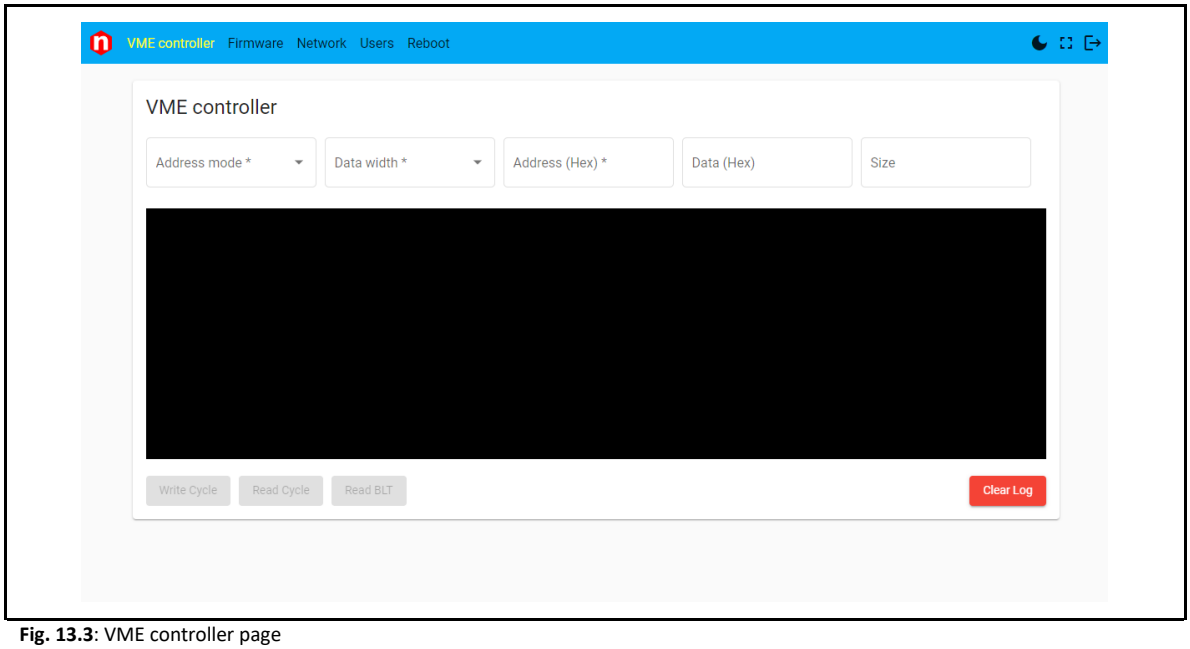


Fig. 13.3: VME controller page

This page allows the User to read/write specific registers of a VME module inserted in the same crate of the V4718, accessing them via VME communication bus. More precisely, the User can define the following information:

- "Address mode": The available options for this parameter are A32, A24, A16.
- "Data width": This parameter indicates on how many bits the content of the register should be written. The available options are D64, D32, D16, D8.
- "Address (Hex)": The address of the register the User would like to access, written in hexadecimal.
- "Data": The data the User would like to write on the content of a specific register, written in hexadecimal.

- "Size": The size, i.e. the number consecutive access to register, required by the User when performing a Block Transfer read (see below).

Once the necessary parameters described above have been filled with a value by the User, the following actions can be performed by pressing the corresponding buttons in the bottom part of the VME controller page:

- "Write Cycle": Allows the User to write down on the selected register the value reported inside the "Data" field (see above). The User can check that the value has been correctly written by performing immediately after a "Read Cycle" (see below).
- "Read Cycle": Allows the User to read the content of the selected register (via the "Address (Hex)" field).
- "Read BLT": Allows the User to perform a Block Transfer read with a number of accesses to register determined by the "Size" parameter.

Firmware update

The Firmware update page allows the User to visualize the current CUP and VME firmwares (refer to Chap. **16** for more details) installed on the V4718 board as well as to upgrade them.

According to **Fig. 13.4**, the firmware releases installed on the V4718 module are:

- CUP firmware rel. 2021052600,
- VME firmware rel. 3.02.

Fig. 13.4: Firmware update page

Upgrade Procedure

- Press the "Browse" button in the Firmware update page (see **Fig. 13.4**) in order to point the firmware file.
- Press the "Update" button to start the upgrade.

The firmware update may take up to few minutes and during that time the status of the dataway display LEDs will be the same as that described in Sec. **Power-on Status**.

Note: The User must not turn off the crate where the V4718 is inserted while the firmware upgrade is in progress.

As soon as the firmware update is finished, a message is displayed telling the User that a reboot is required to restart the V4718 board with the updated firmware loaded.

Note: After the firmware upgrade the reboot must be power cycling the crate.

Network

The Network page allows the User to visualize the network configuration of the V4718 board and to modify it according to the User needs.

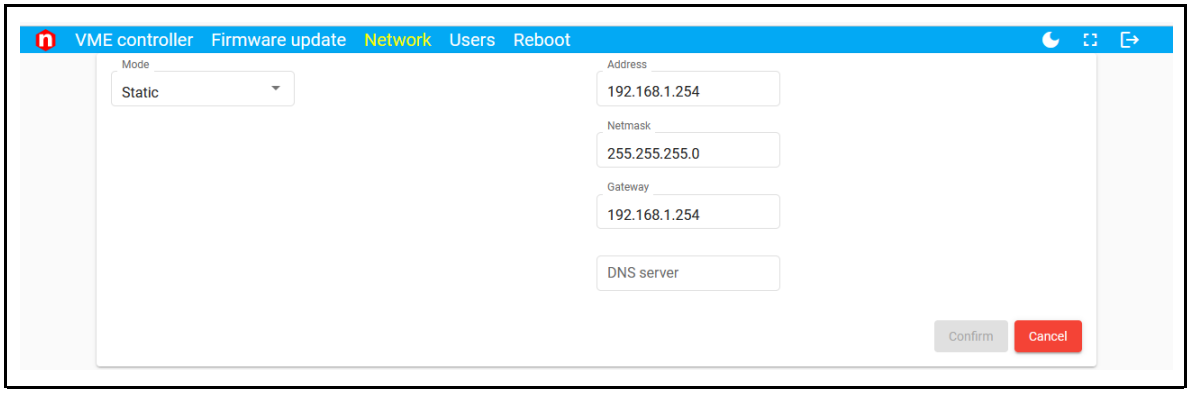


Fig. 13.5: Network page

Inside the Network page, the User can modify the IP Address method (Static/DHCP), the IP address of the board, the Netmask and other settings according to the characteristics of the network.

Note: The User must press the Confirm button and then Reboot the V4718 board to make all the changes to the V4718 network settings effective.

Users

The Users page allows the User to define the settings necessary to login inside the web interface.

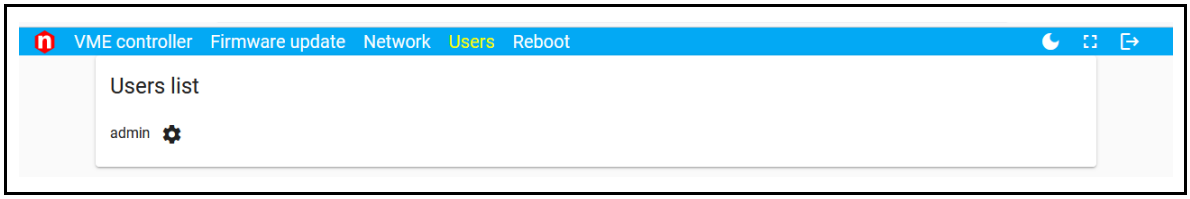


Fig. 13.6: Users page

The User can change the password to access the web interface by clicking on the wheel near the admin label (see **Fig. 13.7**).

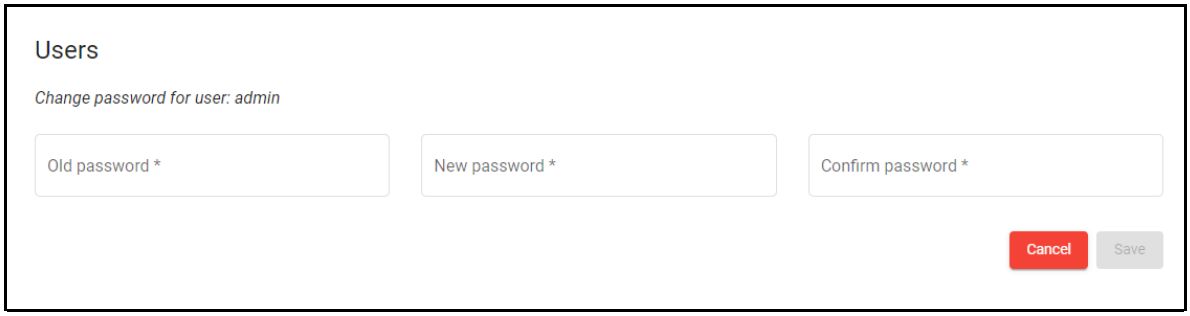


Fig. 13.7: Users page with the fields to change the password

Reboot

The Reboot button allows the User to reboot the board. This button can be particularly handy when the User is upgrading the firmware or changing the network settings and need to reboot the board in order to make the changes effective. When pressing the Reboot button, a dialog box similar to that shown in **Fig. 13.8** is displayed.

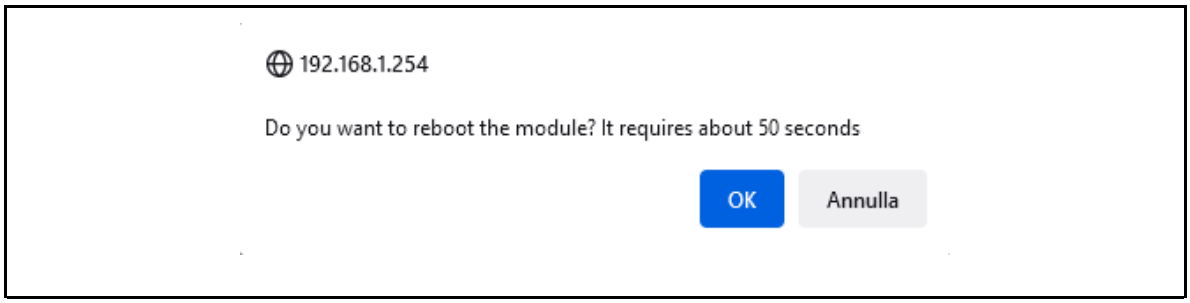


Fig. 13.8: Reboot dialog box.

During the reboot, the board status is the same as that described in Sec. **Power-on Status.** Once the reboot is finished, the Login to the web interface is again required (see Sec. **Login**).

14 Zynq UltraScale+ SoC

The V4718 is equipped with a Zynq Ultrascale+ SoC module including an ARM-based processor running Debian GNU/Linux OS. The system is mainly used to manage both the Ethernet and USB communication links. However, by taking advantage of an Ethernet connection to the V4718 module, the User can access via SSH protocol the SoC module and develop his/her own software on the OS installed, as if it were a PC with a Linux OS installed.

Note: ARM-based processors have much lower computational power than normal PCs. Running softwares requiring high computational capability on the embedded SoC could drastically reduce the overall performance of the entire V4718 module.

Inside the Linux OS of the on-board Soc, the CAENVMEDemo is already present (see Sec.

CAENVMEDemo). This is a simple demo written in C/C++ code based on the functions of the CAENVMELib (refer to Sec. **VMELib Library** and **[RD4]**) and is intended to demonstrate how to control CAEN VME Bridges giving to Users a starting point for the development of their applications.

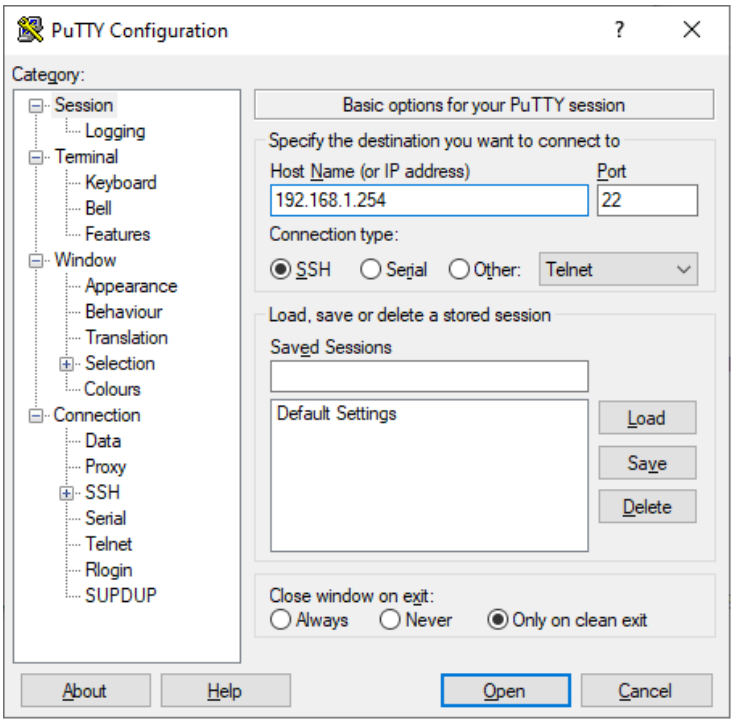
How to Access the Embedded OS

It is possible to access the Linux OS installed on the SoC only by performing an Ethernet connection to the V4718 module and using an SSH protocol. In order to establish an Ethernet connection between the PC and the V4718 module, the User is kindly suggested to check all the instructions reported in Sec. **Ethernet Configuration**. In the following sections, it will be assumed that a point-to-point connection has been previously established between the PC and the V4718 and that the IP address of the V4718 board is the default one, i.e. 192.168.1.254.

Windows OS

In order to establish a connection via SSH protocol on Windows, the User should install a third-party SSH client, e.g. PuTTY as in the example described below.

1.

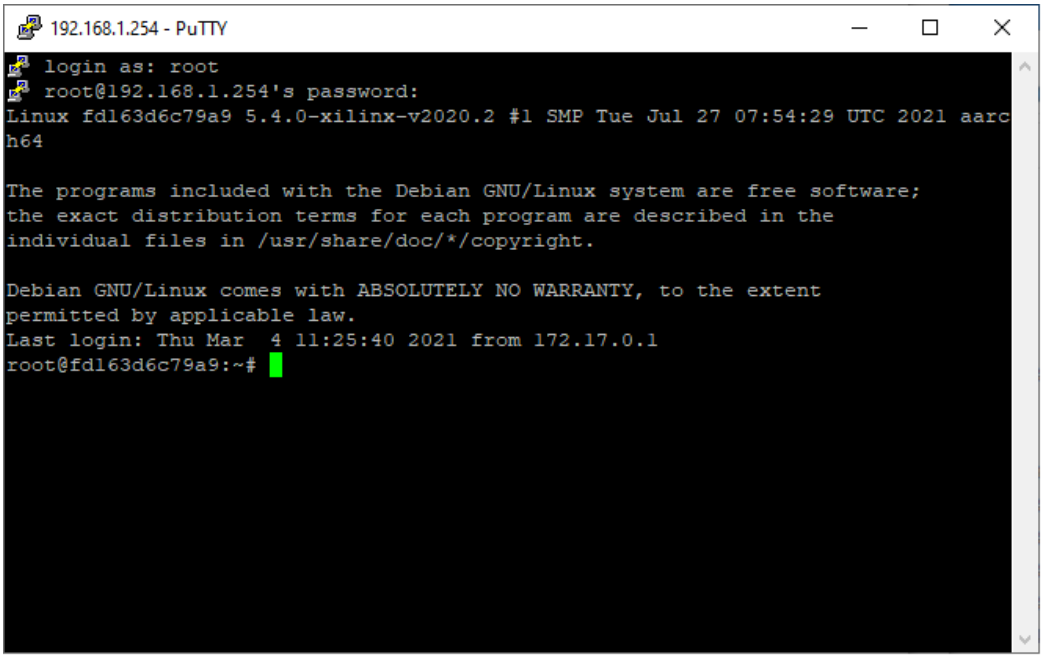


- Open the PuTTY application or another SSH client.
- Insert the IP address of the V4718 module, in this case 192.168.1.254, in the Host Name/IP address field.
- Keep the default access Port, i.e. 22, and put a thick on the SSH option for the Connection type.
- Click on Open.

2.

- A window similar to the one in the figure above will open. The user should use the following credentials:
    - Login as: *root*
    - Password: *root*

3.

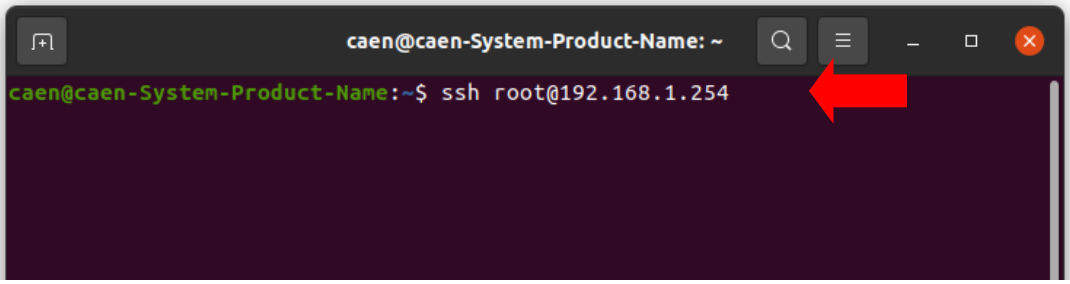


- Once the connection is established, the window opened will be similar to the one in the figure above. The User can visualize information regarding the OS installed on the ARM processor.

Linux OS

In order to establish a connection via SSH protocol on Linux, no third-party software installation is necessary.

1.

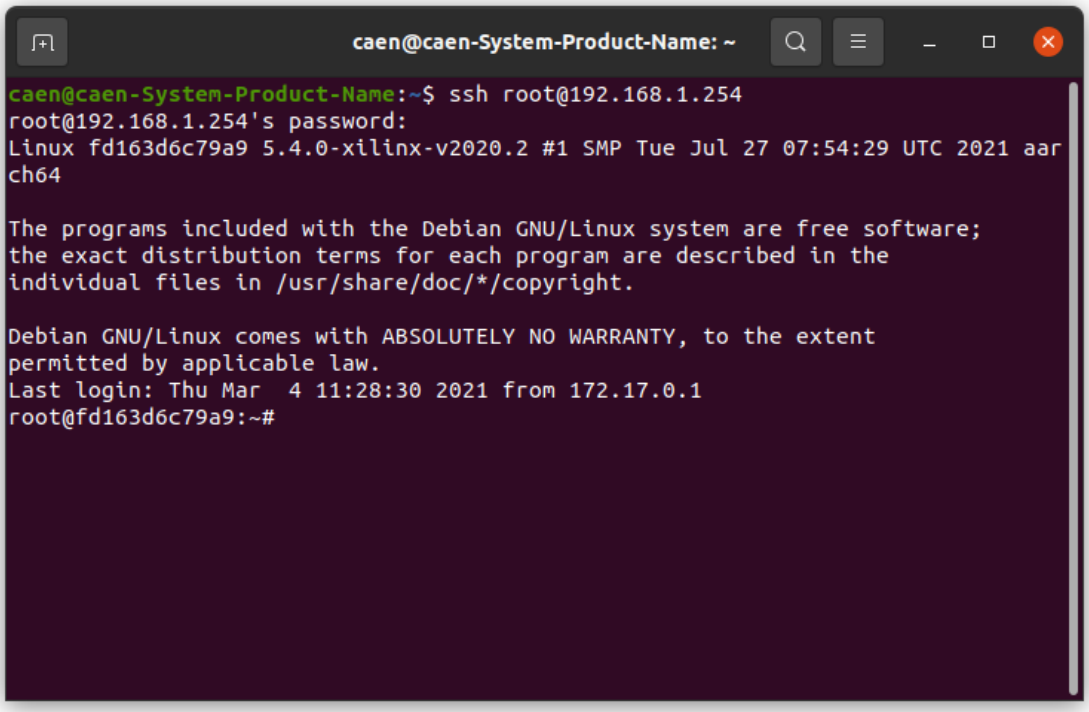


- Open the terminal and type in the command line:

  ssh root@IP address

  With the IP address being 192.168.1.254 in this case.

2.



- Type in the following password to access via SSH: *root*
- The SSH connection is now established. The User can visualize information regarding the OS installed on the ARM processor.

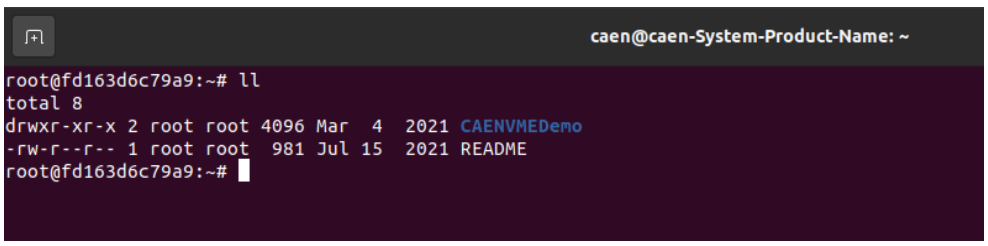
CAENVMEDemo

Once the SSH connection to the Debian GNU/Linux OS installed in the V4718 SoC is established, the User can install all the softwares necessary for its purpose. In case the User software is intended to control the bridge functionality or to access via VME bus the modules present in the same VME crate where the V4718 is installed, an handy starting point is provided by the CAENVMEDemo, which is factory installed in the V4718 embedded Linux OS.

Note: ARM-based processors have much lower computational power than normal PCs. Running softwares requiring high computational capability on the embedded SoC could drastically reduce the overall performance of the entire V4718 module.

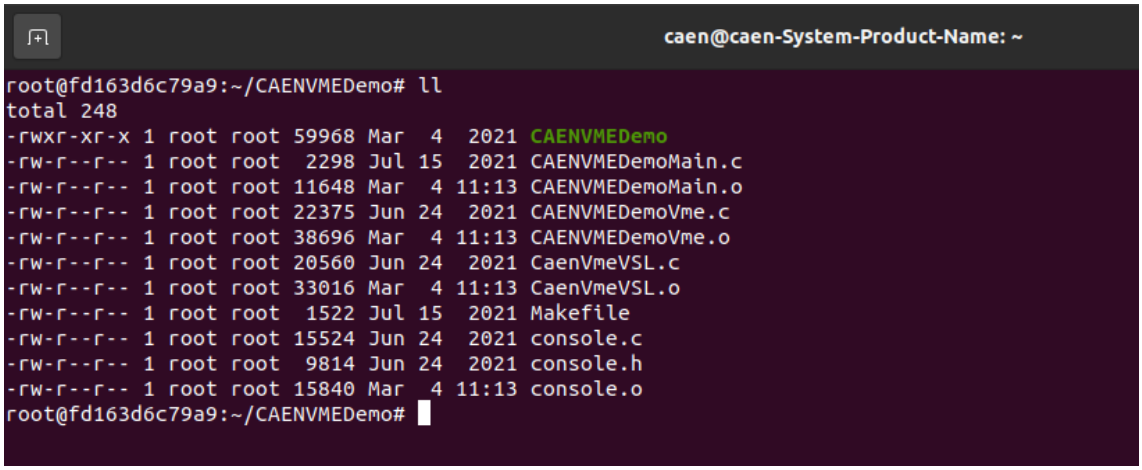
The CAENVMEDemo can be accessed from the location that opens immediately after having established a connection via SSH protocol (see Sec. **How to Access the Embedded OS**).

1.



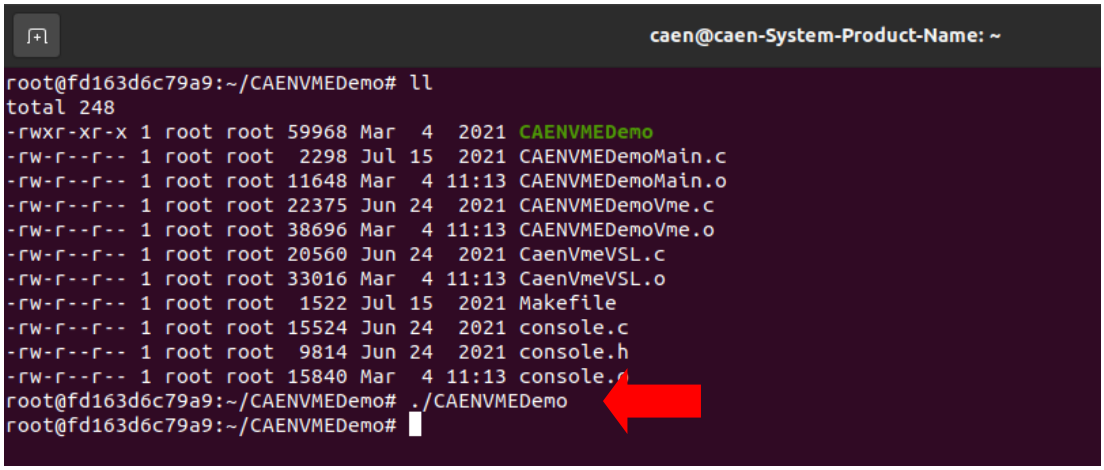
- The User can visualize the presence of the CAENVMEDemo folder and of the corresponding “README” file.

2.



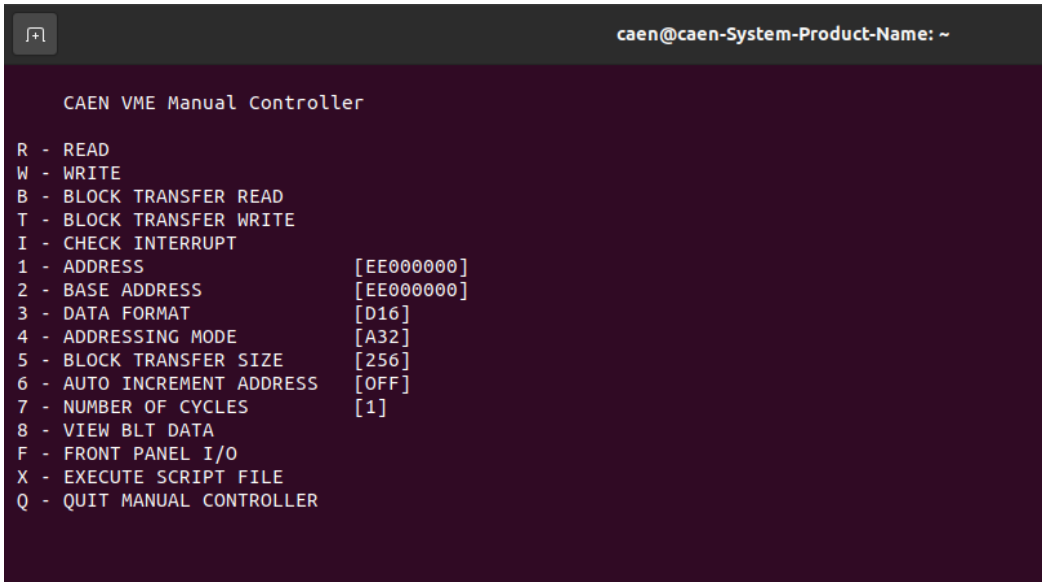
- Enter inside the CAENVMEDemo folder and execute “make”.
- The CAENVMEDemo application is created.
- The User can check the content of the folder once the “make” command has been executed.

3.



- To execute the CAENVMEDemo simply execute the “./CAENVMEDemo” command.

4.



- The CAEN VME Manual Controller is suddenly opened, allowing the User to access the registers of a particular VME module (slave) via VME bus.

15 Software

VMELib Library

CAENVMELib is a set of ANSI C functions helpful for a User software development to configure and control CAEN Bridges V1718, V2718, V3718 and V4718 **[RD4]**.

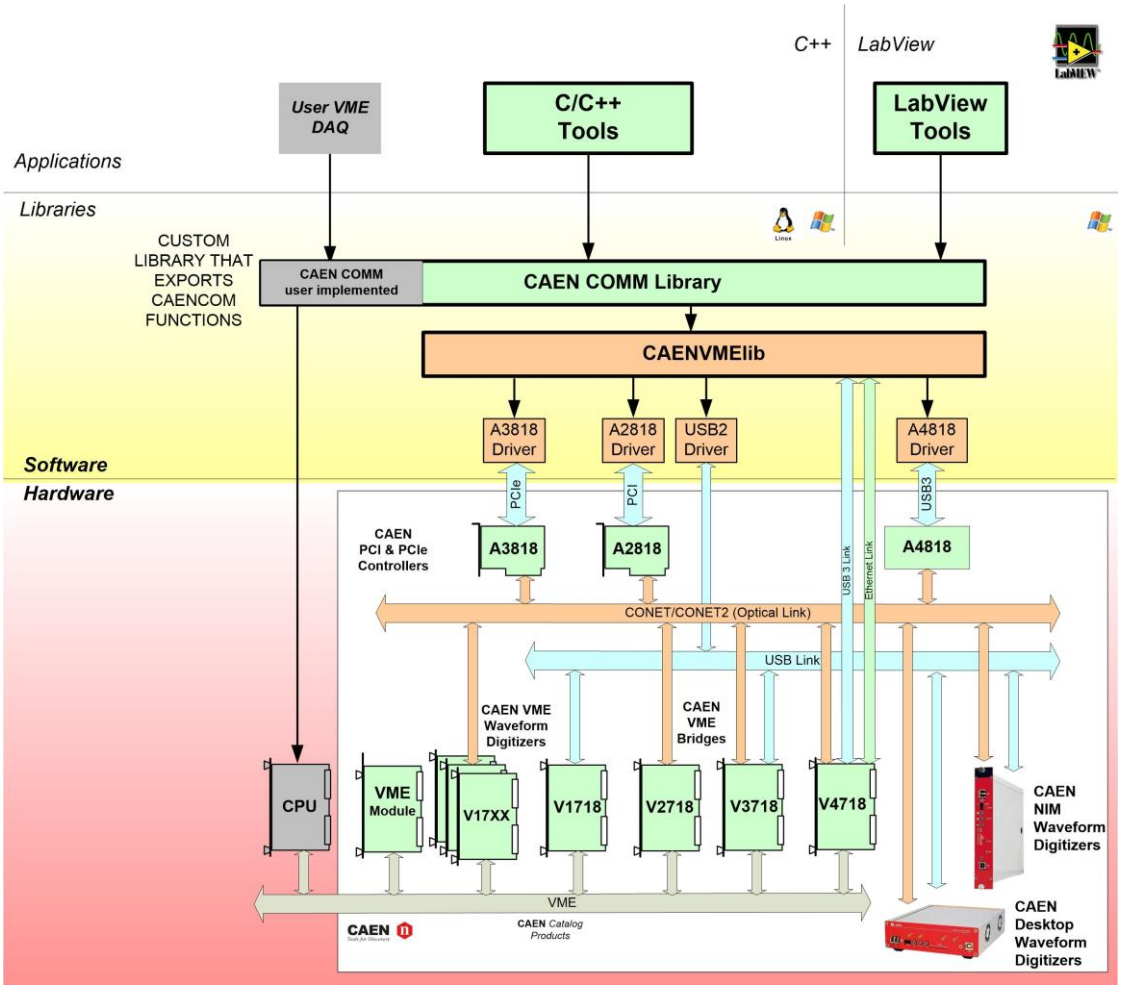


Fig. 15.1: Scheme of CAEN hardware and software layers.

CAENVMELib is logically located between a software application (e.g. sample codes provided by CAEN or user developments) and the lower layer software libraries.

THE V4718 CAEN BRIDGE IS SUPPORTED FROM CAENVMELib LIBRARY REV.3.3 ON

CAENUpgrader

CAENUpgrader is a software composed of command line tools together with a Java Graphical User Interface.

On the V4718, CAENUpgrader allows in few easy steps to perform the following actions:

- Upgrade the VME firmware (see Chap. **16**).
- Read out the current VME firmware revision number.

The User should refer to Chap. **16** for the instructions necessary to perform the actions above.

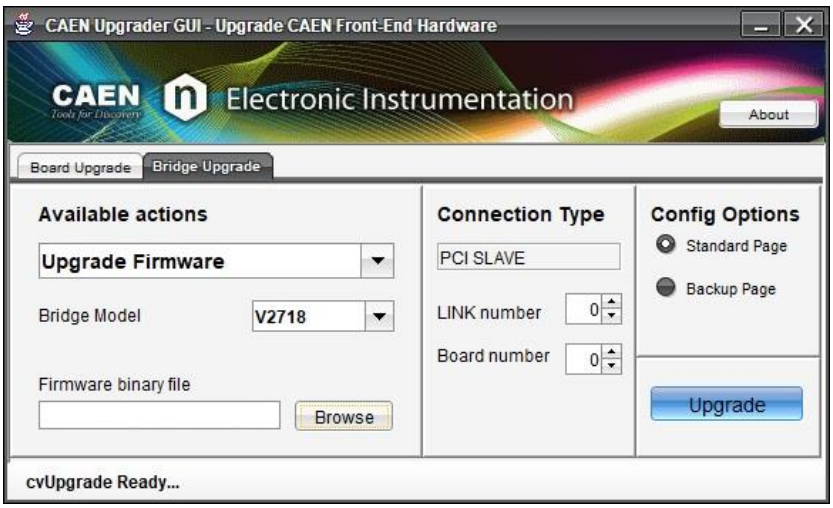


Fig. 15.2: CAENUpgrader Graphical User Interface

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems. The User must also install the required third-party Oracle Java RE 8 u40 or higher.

CAENUpgrader for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVME and CAENCOMM libraries to be installed apart by the User.

Refer to the CAENUpgrader documentation for installation instructions and for a more detailed description **[RD1]**.

16 Firmware and Upgrades

The V4718 module contains two FPGAs:

- An Artix®-7 FPGA allowing the management of the optical interface, of the communication via VME bus and of the board I/Os (see **Fig. 2.1**).
- The FPGA contained inside the Zync UltraScale+ SoC and allowing the management of the communication via Ethernet and USB links and the interfacing with the Artix®-7 FPGA (see **Fig. 2.1**).

The file containing the firmware of the Zync UltraScale+ SoC FPGA is a CUP file, which is an archive of files including the firmware for all the programmable components present on the Zync UltraScale+ SoC, i.e. FPGA and CPU. By upgrading the CUP file, all these components are upgraded at once. The standard name of the CUP file is:

<cup-firmware-version>.CUP

From now on, we will refer to the firmware loaded inside the Zync UltraScale+ SoC as "CUP firmware". We will instead refer to the firmware loaded inside the Artix®-7 FPGA as the "VME firmware", since it manages the VME bus communication. The standard name of the VME firmware file is:

<model>_<vme-firmware-version>.BIN

Where:

<model> is the bridge model

<vme-firmware-version> is the VME firmware revision

The FPGA firmwares are stored onto the corresponding on-board FLASH memories of the two V4718 FPGAs. More precisely:

- The FLASH memory page of the Artix®-7 FPGA is divided into three main pages called Standard, Backup and Factory. Each page stores a copy of the firmware that could not necessary be the same revision number. In normal conditions, at power-on, a microcontroller reads the FLASH memory and automatically programs this FPGA by loading the VME firmware copy stored in the Standard page of the FLASH. The Standard page of the FLASH can be accessed by the user in read and write mode. The Backup page can also be accessed by the user in read and write mode, but it is suggested to use this page only in case of failure of the Standard. The Factory page is accessible in read-only mode as it contains a copy of the VME firmware delivered with the module and intended exclusively for recovery usage if both the Standard and the Backup pages are in a fail status (see Sec. **Troubleshooting**).

IT IS STRONGLY SUGGESTED TO OPERATE THE BRIDGE UPON THE STANDARD COPY OF THE VME FIRMWARE!

THE USER IS RECOMMENDED TO MAKE UPGRADES ONLY ON THE STANDARD PAGE OF THE FLASH!

- The FLASH memory page of the FPGA within the Zync UltraScale+ SoC is divided into two main pages called Standard and Factory. Each page stores a copy of the firmware that could not necessary be the same revision number. In normal conditions, at power-on, a microcontroller reads the FLASH memory and automatically programs this FPGA by loading the firmware copy stored in the Standard page of the FLASH. The Standard page of the FLASH can be accessed by the user in read and write mode. The Factory page is accessible in read-only mode as it contains a copy of the firmware delivered with the module and is intended exclusively for recovery usage if the firmware stored in the Standard page is somehow corrupted.

Firmware File

Firmware updates are available for download at the V4718 page after having logged in to the CAEN website (www.caen.it). The file containing the firmware of both V4718 FPGAs is a CUP file with a name structure as described below:

XXXXYYZZRR.CUP

Where XXXX is the year the file was released, YY the month, ZZ the day and RR the revision.

The VME firmware is a binary (.BIN) file with a name structure as described below:

V3718-V4718_revX.Y.BIN

where V3718 and V4718 indicate with which bridge models that firmware version is compatible, while X.Y is the "major.minor" revision number.

Firmware Upgrade

The User can upgrade the CUP and VME firmware files via the dedicated V4718 web interface (see Sec. **Firmware update**) by taking advantage of an USB or Ethernet connection to the V4718 module.

The User can upgrade the VME firmware of the V4718 also by means of the CAENUpgrader software (see Sec. **CAENUpgrader**) if an optical link connection is established between the PC and the V4718. If this is the case, the User should follow the instructions below:

1. Launch CAENUpgrader and open the *Bridge Upgrade* tab.
2. Select "Upgrade Firmware" in the *Available actions* slide menu.
3. Set "V2718" option as "Bridge Model" if the optical connection to the bridge is realized thanks to an A2818 or A3818 controller. In case the optical connection is realized thanks to an A4818 adapter, the User should select the "USB_A4818_V2718" option.
4. Press the Browse button and point to the VME firmware programming file on your PC.
5. Set the connection parameters according to your communication link and hardware setup **[RD1]**.
6. Select Standard Page in the "Config Options".
7. Press the Upgrade button.
8. Wait until the writing process is completed and the software returns a reboot message.
9. Power cycle the board to make the new VME firmware be loaded on the corresponding FPGA.

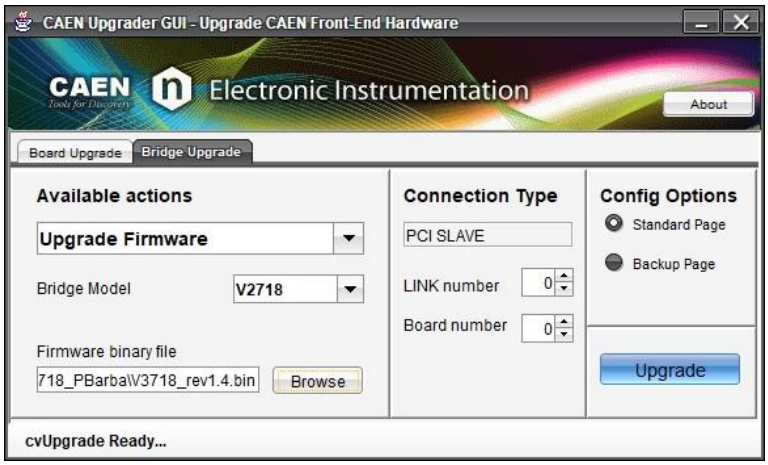


Fig. 16.1: Firmware upgrade settings

WRITING THE VME FIRMWARE ON THE FLASH NORMALLY TAKES FEW MINUTES. A VOLUNTARY INTERRUPTION OF THE PROCESS WHILE IT IS UNDER WAY MAY CAUSE FLASH DAMAGES!

For verification, the user can read out the current VME firmware revision number.

1. Select "Get Firmware Release" in the *Available actions* slide menu.
2. Set "V2718" option as "Bridge Model" if the optical connection to the bridge is realized thanks to an A2818 or A3818 controller. In case the optical connection is realized thanks to an A4818 adapter, the User should select the "USB_A4818_V2718" option.
3. Set the connection parameters according to your communication link and hardware setup **[RD1]**.
4. Press the *Get FW revision* button.

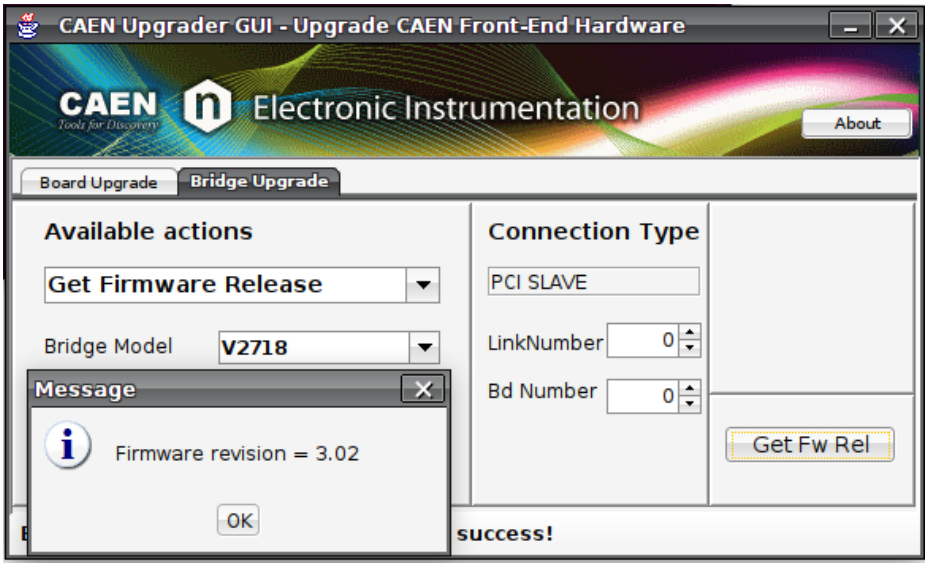


Fig. 16.2: Get Firmware Release settings

Troubleshooting

Usually because of an upgrade failure of the VME firmware, the Standard or/and the Backup pages of the FLASH may be corrupted. In case the communication with the V4718 has been compromised, the User can try to recover by means of the front panel SYSRES button (see Sec. **Front Panel**). If the following attempts fail, please contact CAEN Support (Chap. Errore. L'origine riferimento non è stata trovata.).

Recover from Standard Page Corruption

In this case, it is possible to reboot the Bridge from the Backup page of the FLASH:

- Hold down the SYSRES button and release it as soon the front panel I/O LEDs light on.
- Use CAENUpgrader to load the firmware on the Standard page of the FLASH.
- Reboot the board in Standard mode (no action on SYSRES) and try to read out the firmware revision number for verification.

Recover from Standard and Backup Pages Corruption

When it is not possible to communicate with the bridge neither in Standard nor in Backup mode, it is necessary to enter the Factory mode:

- Hold down the SYSRES button and release it after the front panel I/O LEDs flash off.
- Use CAENUpgrader to load the VME firmware on the Backup page of the FLASH.
- Reboot the board in Backup mode and read out the VME firmware revision number for verification.
- Load the VME firmware on the Standard page of the FLASH.
- Reboot the board in Standard mode and read out the VME firmware revision number for verification.

17 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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